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Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1979 to September 30, 1980

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Semiconductor Materials and Processes Division
Washington, DC 20234

September 1981

Prepared for
Department of Energy
of Electric Energy Systems
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**MEASUREMENT TECHNIQUES FOR
HIGH POWER SEMICONDUCTOR
MATERIALS AND DEVICES: ANNUAL
REPORT, OCTOBER 1, 1979 TO
SEPTEMBER 30, 1980**

R. C. Larrabee, W. E. Phillips, and W. R. Thurber

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

Table of Contents

	Page
Executive Summary	1
1. Introduction	5
2. Characterization of Deep Levels	6
2.1 Task Objectives	6
2.2 Background	6
2.3 Accomplishments During Reporting Period	7
2.3.1 Deep-Level Transient Spectroscopy Measurements	7
2.3.1.1 Modifications to the DLTS Measurement Facility	8
2.3.1.2 DLTS Measurements of Sulfur-Doped Silicon	8
2.3.1.3 Modeling of DLTS Curves	16
2.3.2 Isothermal Transient Capacitance Measurements	20
2.3.2.1 Description of ITCAP System	20
2.3.2.2 ITCAP Measurements of Sulfur-Doped Silicon	22
2.4 Conclusions and Recommendations	25
3. Correlation to Device Performance	28
3.1 Task Objectives	28
3.2 Background	28
3.3 Accomplishments During Reporting Period	29
3.3.1 DLTS Measurements of High-Voltage Rectifier Material	29
3.3.2 Modeling Lifetime in Terms of DLTS Parameters	32
3.3.2.1 Modeling Excess-Carrier Recombination Through Deep Levels	33
3.4 Conclusions and Recommendations	35
4. Standardization Activities for Spreading Resistance on Thyristor-Grade Silicon	37
4.1 Task Objectives	37
4.2 Accomplishments During Reporting Period	37
5. Other Activities Related to DOE-Sponsored Work	38
5.1 Informal Gold-in-Silicon Round Robin	38
6. References	40
Appendix	42

List of Figures

		Page
2-1.	Schematic diagram of the DLTS system	9
2-2.	DLTS curves of five specimens implanted with ^{32}S and a control specimen	11
2-3.	DLTS curves of two specimens diffused with sulfur at 1350°C . .	13
2-4.	Comparison of the DLTS curves of two silicon specimens doped with sulfur by implantation and one specimen doped by diffusion	14
2-5.	DLTS curves showing the effects of annealing on a specimen from wafer 87A	15
2-6.	Comparison of the calculated experimental DLTS curve for a specimen from an n -type silicon wafer doped with platinum . . .	18
2-7.	Comparison of calculated and experimental DLTS curves for a specimen from wafer 87A implanted with sulfur	19
2-8.	Schematic diagram of ITCAP system	21
2-9.	ITCAP emission time constant as a function of distance from the diode junction for ^{34}S and ^{32}S defect centers at two different average electric field densities	24
2-10.	ITCAP response at 129.8 K for a ^{32}S implanted diode before and after annealing for 5 h at 550°C	26
3-1.	DLTS curve of a p - n junction test diode fabricated on n -type high-voltage rectifier material	30

PREFACE

This work was conducted as a part of the Semiconductor Technology Program at the National Bureau of Standards (NBS). This program serves to focus NBS research in order to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of Government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems of the Department of Energy (DOE) under DOE Task Order AO21-EES. The contract was monitored by Dr. Russell Eaton of DOE. The NBS point of contact for information on the various task elements of this project is R. D. Larrabee of the Semiconductor Materials and Processes Division (formerly part of the Electron Devices Division) at the National Bureau of Standards.

The authors wish to acknowledge the work of Brenda Kefauver in preparing the manuscript of this report and to thank W. M. Bullis and R. A. Forman for many stimulating technical discussions.

Measurement Techniques for High Power
Semiconductor Materials and Devices

ANNUAL REPORT

October 1, 1979 to September 30, 1980

R. D. Larrabee, W. E. Phillips, and W. R. Thurber

EXECUTIVE SUMMARY

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from the rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes. Application of this measurement technology will, for example, enable industry to make devices with higher individual power-handling capabilities, thus permitting reductions in the cost of power-handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major effort under this continuing project is to determine procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce lifetime or contribute to leakage current in power-device grade silicon. This effort is divided into two ongoing tasks concerned with (1) the introduction of specific impurities into silicon wafers and the characterization of the resulting deep levels and (2) the correlation of the results of these deep-level characterization techniques with the electrical properties of devices. A third task concerned with the standardization of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon was essentially completed during the year.

The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during crystal growth and during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. In either case, the dominant effect of the deep level is to modify the excess-carrier lifetime. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The use of such techniques for process diagnostics would enhance the manufacturer's ability to control the quality (yield, reliability, and cost) of his product. The effective utilization of deep-level measurements requires three things: (1) developing well-characterized measurement and data

analysis procedures, (2) characterizing a variety of levels to establish the validity of techniques and establishing a data bank of the properties of known defect levels, and (3) understanding the relationship between the presence of deep levels and the corresponding device parameters. Efforts in deep levels during this contract period were aimed specifically at the first and third of these basic requirements.

Deep-Level Measurements - During FY-1980, it was discovered that the thermal emission rate (the experimental parameter from which thermal activation energy is derived) is not a unique characterization parameter for the levels observed in sulfur-doped silicon. Specifically, it was found that the thermal emission rate is a function of spatial position with respect to the p - n junction of the test device, of the thermal processing used in the fabrication of the test device, and of the concentration level of sulfur. This variability with position, thermal history, and density is not expected for a single well-defined energy level in a semiconductor. If sulfur is not exceptional in this regard, such variability may impact the significance, understanding, and value of deep-level measurements for many applications. Therefore, it became critical to confirm these results and to develop better techniques to characterize and to identify the causes of this variability. The initial experiments which revealed this behavior have been repeated, verified, and improved. The previously developed analytical model for predicting the position and shape of DLTS curves has been improved and put into routine use as a tool for interpreting DLTS results. Moreover, various physical characterization techniques have been added to the NBS deep-level task, with the anticipation that they would provide a fundamentally different kind of characterization of the deep-level states and thereby contribute information about the physical nature of these states that is not available by electrical characterization techniques alone.

The variability of thermal emission rate observed for sulfur-doped silicon strongly suggests that the traditional view of sulfur levels as arising from two charge states of a simple substitutional donor is not correct. The available evidence in the literature suggests that this situation is not unique to sulfur, and at this time, it is not known how extensive these effects are. Until this is determined, every level must be suspect, and until resolved, any interpretation of deep-level measurements is open to question.

These results have motivated an interest in finding a counter example - a deep level that does not exhibit these variability effects. A "simple" level such as this would also be a promising candidate for a standard DLTS test specimen and a starting point for double-doping experiments designed to reveal the variability effects associated with impurity-complexing phenomena (the mechanism currently thought to be responsible for the variability observed in sulfur-doped silicon). Some tentative results obtained to date indicate that platinum may introduce such a simple level into silicon. If future research proves this to be the case, platinum-doped silicon

will become a very interesting system to study for a variety of theoretical and practical reasons.

Correlation to Device Performance - Deep-level defects in the silicon bandgap play an important role in determining the behavior of high-power devices. These defects, which can be present either intentionally (e.g., to control switching speed), or unintentionally (e.g., introduced by the starting material or by the device processing), control the minority-carrier lifetime in the active regions of devices. To this extent, they control such electrical parameters as reverse leakage current, forward voltage drop, and switching speed. Therefore, it is important to understand the nature of the mechanism of minority-carrier recombination and its effects on relevant device parameters. One test of the depth of understanding that has been achieved is to determine the degree of correlation between lifetime measurements and the results of modeling the behavior of the excess-carrier lifetime as a function of the measured deep-level characterization parameters. Previous reports have presented the results of experiments where such a correlation was demonstrated qualitatively in specially prepared gold-doped specimens. The present continuing effort is directed at demonstrating this correlation quantitatively in real device material. A computer program is being written for predicting the excess-carrier lifetime of multilevel systems given the density, activation energy, and carrier cross-sections of all the states in the bandgap. However, the variability seen in sulfur-doped silicon portends potential problems in using the traditional deep-level characterization parameters derived from emission-rate measurements in this way. In other words, unless one has carefully ascertained that the levels in question are "simple" and adequately characterized by a unique thermal emission rate at any given temperature, one should seriously question any interpretation of deep-level measurements in terms of activation energies and capture cross sections. Although the techniques developed for studying sulfur-doped silicon can now serve as procedures for testing for variability effects in other systems, it is not clear at this time what to do if the levels in question show variability effects. Therefore, any initial test of understanding based on a correlation between measured and computed excess-carrier lifetime will have to be performed on some system in which the dominant lifetime-determining levels have previously been shown to exhibit a unique thermal emission rate at any given temperature.

Standardization Activities for Spreading Resistance on Thyristor-Grade Silicon - During FY-1980, the task to increase the reliability with which spreading resistance measurements can be used for radial resistivity screening of thyristor substrate material and for depth resistivity profiling of partially or fully fabricated thyristor structures was essentially completed. The formal acceptance procedure within ASTM of the standard practice for preparing high-resistivity *n*-type silicon for spreading resistance measurements was completed with a Society-level ballot in May. This Standard Practice was published in Part 43 of the *Annual Book of ASTM*

Standards and has the designation F 674-80. (See also Appendix A of this report.)

Six of the 15 laboratories participating in the interlaboratory program to determine the repeatability of spreading resistance measurements on bulk silicon specimens have completed their measurements. Analysis of these data, emphasizing repeatability as a function of specimen preparation, is being undertaken under NBS sponsorship and the results included in a future DOE report.

Interlaboratory Round Robin - Several firms in the power-device industry have expressed an interest in having NBS issue a well-characterized standard deep-level specimen that could be used to validate the many different transient capacitance systems throughout the world and thereby minimize equipment calibration errors in reported deep-level measurements. As a first response to this need, NBS has been conducting a round-robin interlaboratory test on the same deep-level test device to obtain an estimate of the magnitude of any measurement problems in the field. The results from six laboratories obtained to date show a standard deviation of about 3 percent in reported activation energies and thus indicate a precision adequate for many industrial, but not all research, purposes.*

* This level of precision requires careful attention to thermometry and was not always initially obtained. When this level of precision was not obtained, it was recognized and the thermometry improved. The precision of the new results increased significantly.

1. INTRODUCTION

This project is directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electric power and from the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes.

The project is designed to provide, disseminate, and foster the standardization of improved measurement methods required in high-power semiconductor technology, for use in specifying materials and devices in commerce, and for use by industry in controlling device manufacturing processes and in designing systems. Application of this measurement technology will, for example, enable industry to: (1) make power semiconductor devices with greater uniformity of characteristics, thus permitting improvements in parallel and series connections of devices for applications from fusion-energy generation to ac/dc conversion; (2) make devices with higher individual power-handling capabilities, thus permitting reductions in the cost of power-handling equipment and fostering the development of dc transmission lines to reduce both energy waste and the extent of required rights-of-way; and (3) provide devices, and the systems utilizing them, with the reliability and performance required in energy generation, utilization, and conservation.

The major effort under this continuing project is to determine procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce excess-carrier lifetime or contribute to leakage currents in power-device grade silicon. This effort is divided into two ongoing tasks concerned with (1) the introduction of specific impurities into silicon wafers and the characterization of the resulting deep levels and (2) the correlation of the results of these deep-level characterization techniques with the electrical properties of devices. A third task concerned with the standardization of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon was essentially completed during the present reporting period.

2. CHARACTERIZATION OF DEEP LEVELS

2.1 Task Objectives

The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during crystal growth and during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. In either case, the dominant effect of the deep level is to modify the excess-carrier lifetime. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The use of such techniques for process diagnostics would enhance the manufacturer's ability to control the quality (yield, reliability, and cost) of his product. The effective utilization of deep-level measurements requires three things: (1) developing meaningful and well-understood measurement and data analysis procedures, (2) characterizing a variety of levels to establish a data bank of the properties of known defect levels, and (3) understanding the relationship between the presence of deep levels and the corresponding device parameters. This section of the report will be concerned with the first item and section 3 will be concerned with the third item. The second item cannot be effectively undertaken until the first item has been completed.

The emphasis of this continuing task is to introduce known impurities into silicon and to validate the measurement of their deep-level characterization parameters in order to determine their uniqueness and utility as material characterization parameters. The ultimate goal of this work would be the development of a badly needed standard test specimen and a catalog of well-characterized deep-level states.

2.2 Background

Sulfur-doped silicon was initially selected as a test vehicle for developing our deep-level measuring capability and for testing our understanding of the results of such measurements. Sulfur was selected on the basis of ease of specimen preparation (by implantation and diffusion of sulfur into the specimen) and with the anticipation that sulfur would occupy a substitutional position in the silicon lattice and act as a simple double-donor type of deep level. However, almost immediately, some significant unexpected results were obtained. A specimen prepared with sulfur of mass 34 had a 14-meV difference in the measured thermal activation energy of the deeper level compared to a specimen prepared with sulfur of mass 32 [2-1,2-2]. The existence of an isotope-related difference this large would indicate an otherwise unsuspected degree of vibronic coupling between the electronic states of the sulfur center and the silicon lattice [2-2]. In addition, the two sulfur levels thought to arise from two different charge states of the same sulfur center had the expected equal density in some specimens, but significantly different densities in other specimens [2-3,2-4]. These results motivated an interest in developing other techniques which could circumvent some of the limitations of the electrical techniques and thereby provide additional information about these sulfur levels in silicon. One of these limitations is resolution, because the thermal excitation mechanism in the electrical measurement is not

very selective and cannot resolve closely spaced levels. This motivated an experiment to measure the resonant infrared absorption between the ground state and the first excited state of the deeper sulfur level and thereby to confirm or deny the electrically observed isotope-related variation.* The results of this optical experiment [2-5] were significant in two ways. First, the isotope-related difference observed by the optical technique was about two orders of magnitude lower than the electrically observed value of 14 meV. Second, a number of side peaks of unknown origin were observed close to, but distinctly different from, the main (largest) infrared absorption peak. Both the main peak and the side peaks were absent in control specimens processed the same way, but without any sulfur. In addition, all these peaks decreased in amplitude with annealing of the specimen in an inert atmosphere at 550°C for several hours. However, the rate of decrease in amplitude was not the same for all the peaks. These results indicated that all these peaks are related to the presence of sulfur, but do not arise from the same sulfur center [2-5]. The existence of different sulfur-related centers coupled with the unexpected electrical results implies a degree of complexity, an inadequacy of understanding, and a lack of control and casts doubt not only on the interpretation of previous electrical experiments, but also on the conventional viewpoint of sulfur as a simple substitutional double-donor deep level in silicon.

A possible explanation of these results is that there is no single sulfur center, but a multiplicity of sulfur-related centers [2-5] such as might be caused by complexing of the sulfur with itself, with other impurities, or with structural defects. If the multiple peaks observed in the optical measurements are directly attributable to different complexes, they would not be so resolved in electrical deep-level measurements and would collectively contribute to what would appear to be a single peak. Changes in the relative population of multiple centers such as might be caused by annealing, different residual impurities in different specimens, etc., would result in variations in the unresolved (or average) electrical characteristics of the apparent single peak. Experiments demonstrating this behavior are discussed in the following section. Taken together, these optical and electrical results support one another and raise serious questions about the adequacy of the present understanding of deep levels in silicon in general, and about the conventional interpretation of the results of deep-level measurements in particular.

2.3 Accomplishments During Reporting Period

2.3.1 Deep-Level Transient Spectroscopy Measurements

Deep-level measurement techniques such as deep-level transient spectroscopy (DLTS) are based on the ability of electrically active defects to trap free carriers and to re-emit them by thermal stimulation. Analysis of the measured thermal emission rate into the depletion layer of a test device as a

* This work of R. A. Forman was an exploratory project within the NBS Semiconductor Technology Program that was not directly supported by DOE and has been independently reported in *Applied Physics Letters* [2-5]. The key results are summarized here to explain the background and motivation of the present program.

function of temperature gives the activation energies of the defects present. The magnitude of the changes of the capacitance of the depletion layer associated with this emission can be related to the densities of the defects present. One advantage of DLTS as compared to alternative deep-level characterization techniques is its ability to provide quickly a graphical picture of the density and approximate relative position in energy of the electrically active deeper levels in the bandgap of a semiconductor. The system developed at NBS for DLTS measurements was discussed in considerable detail in last year's DOE annual report [2-6]. This system has been improved and used to study the properties of the sulfur-related centers in silicon. This work, which is discussed below, not only demonstrates the electrical effects in sulfur-doped silicon that were suggested by the earlier optical work, but also has evolved to the point where the techniques developed to study sulfur can be used to search for similar behavior in other impurity systems, and thereby determine how extensive these variability effects really are.

2.3.1.1 Modifications to the DLTS Measurement Facility

A number of improvements were made to the previously described [2-6] DLTS measuring system. One series of modifications was designed to simplify the equivalent circuit of the specimen, differential transformer, and compensating impedance (see fig. 2-1), so that the effects of changing specimen impedance could be more easily modeled. A series resistor was added to the compensating side of the differential transformer to enable the system to be balanced more precisely for specimens that contain some series resistance. A potentiometer of 100 Ω has met the range and sensitivity needs for this balance resistance (R_B in fig. 2-1). The variable capacitor (C_B in fig. 2-1), for balancing the capacitance of the test specimen, has a maximum value of 300 pF. The differential transformer was mounted as close as possible to the specimen probe to minimize stray capacitance. An emitter-follower circuit was constructed close to the output of the differential transformer to minimize any stray capacitance or loading effects that might otherwise be reflected back through the differential transformer into the measuring circuit. In addition to these changes, an RC filter was placed between the main pulser and the differential transformer to decouple the RF generator from the pulser and the trigger circuits to which it is connected.

During operation, the phase of the reference and transformer output signals applied to the L and R inputs of the double balanced mixer, respectively, are separately monitored on an oscilloscope and the phase shifter in the reference line adjusted so that these signals are in phase for a capacitive unbalance. In addition, the values of specimen capacitance and series resistance are estimated from the settings of the compensating capacitance and resistance under balanced conditions. Theoretical check of the equivalent circuit is then made to assure that changes in admittance of the specimen due to changes in specimen capacitance (ΔC) at the operating frequency will be linear in ΔC to the accuracy required. The DLTS system shown in figure 2-1 and operated as described was used for all the DLTS results reported below.

2.3.1.2 DLTS Measurements of Sulfur-Doped Silicon

As part of the effort to understand the variability observed in the emission rate from the energy levels associated with sulfur in silicon, DLTS curves

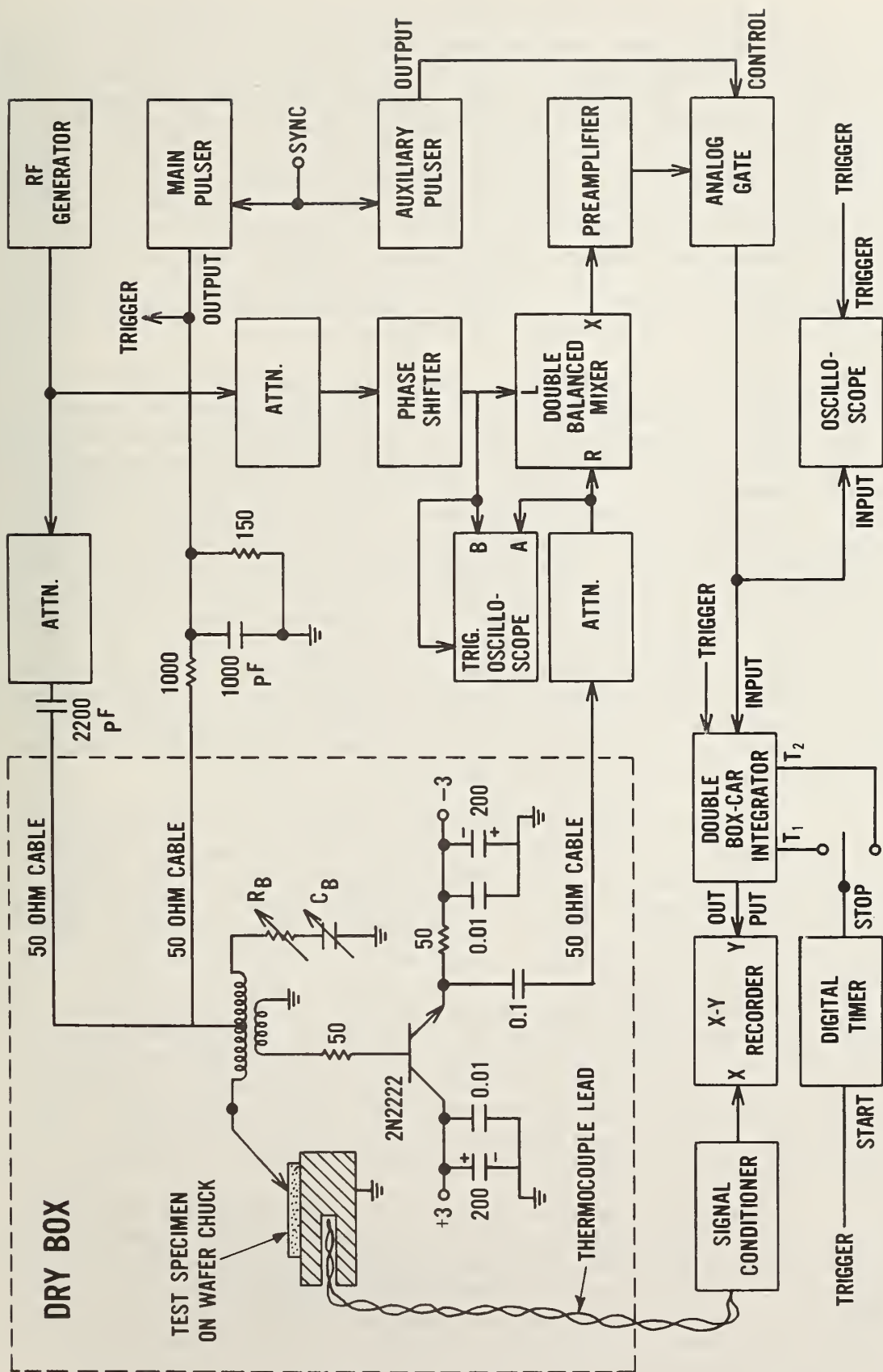


Figure 2-1. Schematic diagram of the DLTS system. Resistances are in ohms and capacitances in μF unless otherwise stated.

were obtained on a number of silicon specimens with a wide range of sulfur densities. Two specimens were heavily doped by diffusion at 1350°C in sealed quartz ampoules. The starting material was 5- to 10- $\Omega\cdot\text{cm}$ n -type silicon with a diffusion time of 22 h for specimen 135B and about 200 h for specimen 8. Both times were long enough for the sulfur to be uniformly distributed and equal to the solid solubility at 1350°C, which is in the low 10^{16} cm^{-3} range. The specimens were quenched by rapidly removing the ampoules from the furnace and plunging them into room temperature water. After diffusion the resistivity of both specimens was about 1 $\Omega\cdot\text{cm}$ (n -type), and spreading resistance measurements indicated very uniform sulfur concentration. Shallow p^+n diodes were fabricated on specimen 135B by ultrasonically applying indium-gallium solder and then heating to 225°C for 15 min. Schottky diodes were fabricated on specimen 8 by evaporating a pattern of aluminum dots.

A group of five additional specimens was prepared by ion implantation of sulfur and subsequent thermal annealing [2-7]. A control wafer which underwent the same thermal processing but without the sulfur implantation was also measured. The devices used for the DLTS measurements on the ion-implanted and control specimens were p^+n junctions (structure No. 19) of test pattern NBS-2 [2-8]. The junctions were fabricated on 5- to 10- $\Omega\cdot\text{cm}$ $\langle 111 \rangle$ n -type silicon wafers prior to sulfur implantation. A 10-min 1000°C anneal in dry nitrogen followed the implant. Then approximately 150 nm of oxide were chemically deposited at 400°C over the junctions. This was followed by a 15-min 1000°C treatment in dry nitrogen to densify the deposited oxide and further diffuse the sulfur. Because sulfur is a relatively fast diffuser, the density in the junction region was approximately proportional to the implanted dose and was uniform as determined by capacitance-voltage (C-V) measurements. Metallization steps completed the fabrication process [2-7]. The control wafer is number 86A and the five ion-implanted wafers are 86B, 86C, 87A, 87B, and 87C (in order of increasing sulfur density).

Figure 2-2 shows the DLTS curves of the control specimen and specimens from each of the five wafers with different densities of implanted ^{32}S . The signal from the boxcar averager, which is the capacitance value of the transient at a sampling delay time of t_1 minus the capacitance value at a delay time of t_2 , is plotted on the vertical axis. The temperature, which is slowly varied at a rate of about 0.1°C per second, is plotted on the horizontal axis. For these curves the delay times were $t_1 = 157\text{ }\mu\text{s}$ and $t_2 = 930\text{ }\mu\text{s}$, giving an effective emission rate window [2-6] peaking at 435 μs . The curves show negative peaks corresponding to the decay of capacitive transients representing electron emission. A DLTS emission peak at low temperatures arises from a relatively shallow energy level, whereas a deep energy level (near the middle of the bandgap) gives an emission peak at higher temperatures. The operating frequency of the capacitance bridge was 20 MHz, the reverse bias was -10 V, and the defects were filled by removing this bias for 100 μs .

Only two DLTS emission peaks are seen in specimens from the three most lightly doped wafers (i.e., 86B, 86C, and 87A), as figure 2-2 shows. The control specimen (from wafer 86A) shows a peak near room temperature within a few degrees of that recorded for the deep level ($\sim 500\text{ meV}$) of sulfur in silicon. The amplitude is about two-thirds the corresponding peak for the lowest dose sulfur-implanted specimen. No response is evident in the control specimen at low temperature in the region corresponding to emission from the shallow

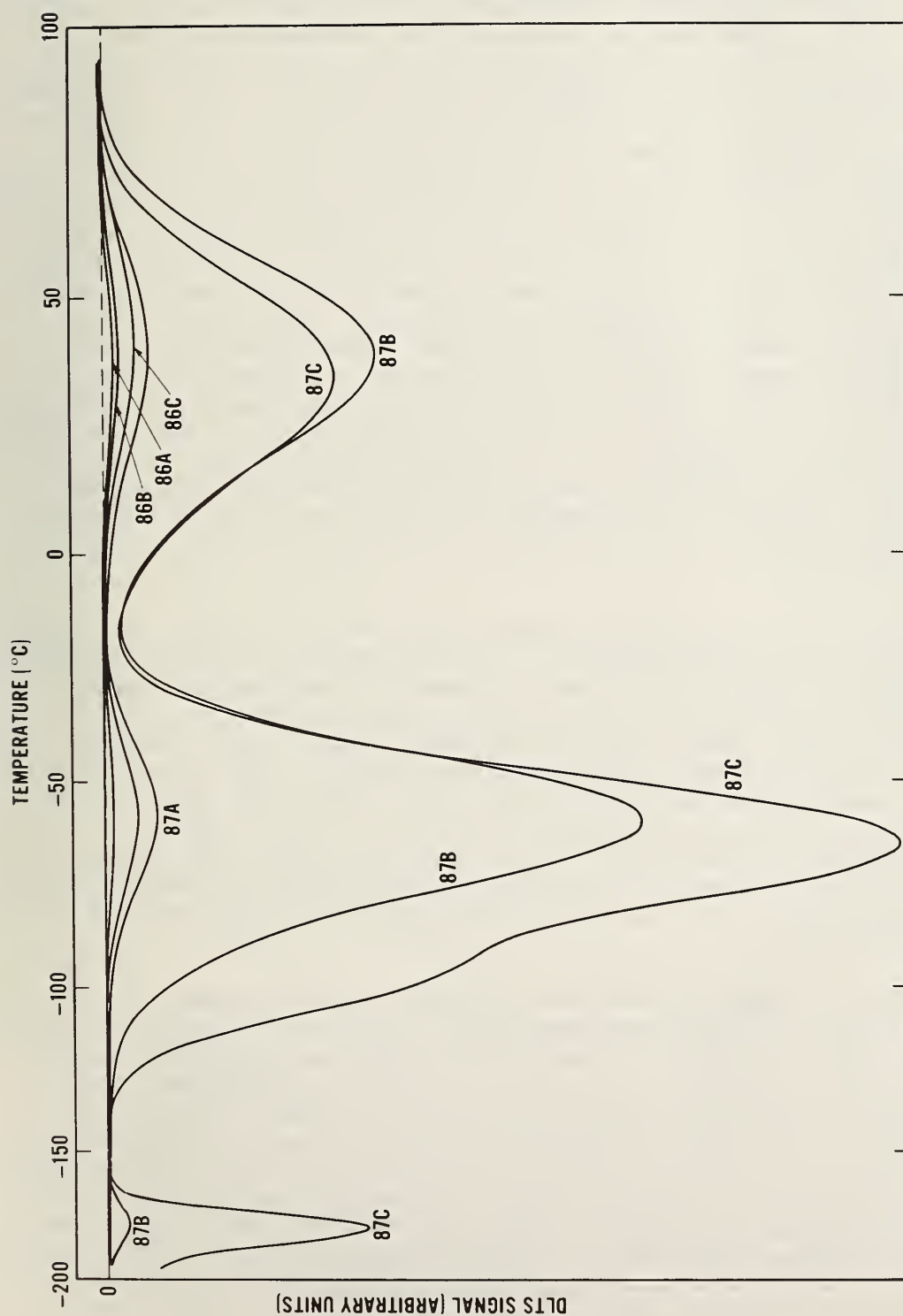


Figure 2-2. DLTS curves of five specimens implanted with ^{32}S and a control specimen. The doses were as follows: 86A, none (control); 86B, $5 \times 10^{13} \text{ cm}^{-2}$; 86C, 10^{14} cm^{-2} ; 87A, 10^{14} cm^{-2} ; 87B, 10^{15} cm^{-2} ; and 87C, $7 \times 10^{15} \text{ cm}^{-2}$. The measurement parameters are given in the text. A negative DLTS signal corresponds to majority carrier (electron) emission.

(~250-meV) sulfur level. Thus the higher temperature peak of the control specimen is not attributed to sulfur. Taking this peak from the control specimen into account, the most lightly doped specimen has about equal intensity in its sulfur-related peaks in agreement with the recent work of Grimmeiss *et al.* [2-9]. As the doping increases, the low-temperature peak increases more rapidly than the room-temperature peak. For an implanted dose of 10^{15} cm^{-2} (wafer 87B), the low-temperature peak has about twice the intensity of the room-temperature peak. This is attributed to the fact that the trap density and the shallow dopant density are about equal in wafer 87A, thus invalidating DLTS peak height as a direct measure of trap density. Both peaks are shifted a few degrees to a lower temperature (an apparent shift to shallower energy levels). In addition, there is a small new peak at a much lower temperature with an activation energy of about 100 meV. With a further increase in implanted dose to $7 \times 10^{15} \text{ cm}^{-2}$ (wafer 87C), the temperature shift continues, and a new level appears as a bump on the low side of the main low-temperature peak. The amplitude of the higher temperature peak actually decreased, whereas that of the other peaks increased with dose as intuitively expected. This work is the first to show systematically how the relative amplitude and position of the two main DLTS peaks of sulfur in silicon change with sulfur concentration. To summarize, for low-sulfur concentration both peaks have about the same amplitude, whereas at high-sulfur concentration the DLTS peak of the shallow level has two to three times the amplitude of the deep level, and both peaks are shifted from their low-concentration positions.

The DLTS curves of the two diffused specimens are shown in figure 2-3 and were obtained using the same parameters as those used for the curves in figure 2-2. Diffused specimen 135B shows the same DLTS peaks as the heavily implanted wafers of figure 2-2 plus one additional small peak at about -140°C. The very large lowest temperature peak, arising from a level at about 100 meV, has been seen before in optical absorption [2-10] and Hall effect [2-11] measurements, but this is the first time it has been seen by DLTS. The other diffused specimen (No. 8) shows the three highest temperature peaks as specimen 135B, but the presence of the lower temperature peaks is uncertain as the series resistance of this specimen is very high at low temperatures which gives rise to poor bridge sensitivity because of the large RC time constant.

The correspondence of peaks between the ion-implanted and diffused specimens is seen more clearly in figure 2-4 where DLTS curves for two implanted wafers of different density (87A and 87C from fig. 2-2) and one diffused specimen (135B from fig. 2-3) are shown. Figure 2-4 strongly suggests that at least three of the peaks are sulfur-related because they are seen in specimens prepared by two very different procedures. These are the lowest temperature peak (corresponding to a level at about 100 meV) and the two highest temperature peaks (corresponding to levels at about 250 and 500 meV). However, this figure also illustrates differences between ion-implanted and diffused specimens, such as relative amplitudes of the peaks, which appear to involve more than just sulfur concentration. For example, the temperature of diffusion and the cooling rate may determine the concentration of each level formed.

Figure 2-5 shows the results of an annealing experiment performed on a specimen from wafer 87A. This work was undertaken because of relative changes in

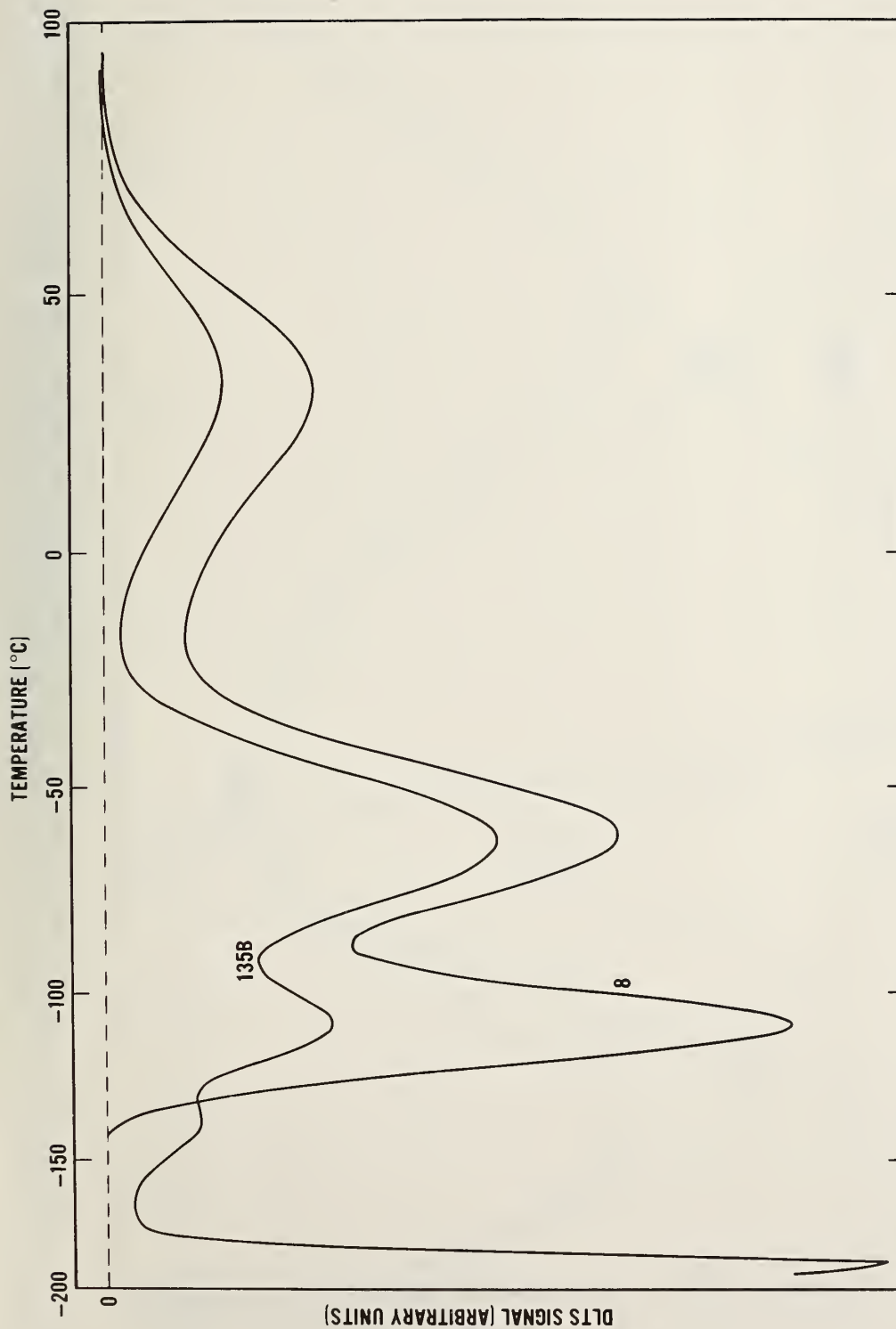


Figure 2-3. DLTS curves of two specimens diffused with sulfur at 1350°C. Specimen 135B was prepared from 5-Ω·cm, *n*-type silicon with a diffusion time of 22 h. The starting material for specimen 8 was 12 Ω·cm, *n*-type silicon, and the diffusion time was about 200 h. The measurement parameters, given in the text, are the same as those used in figure 2-2.

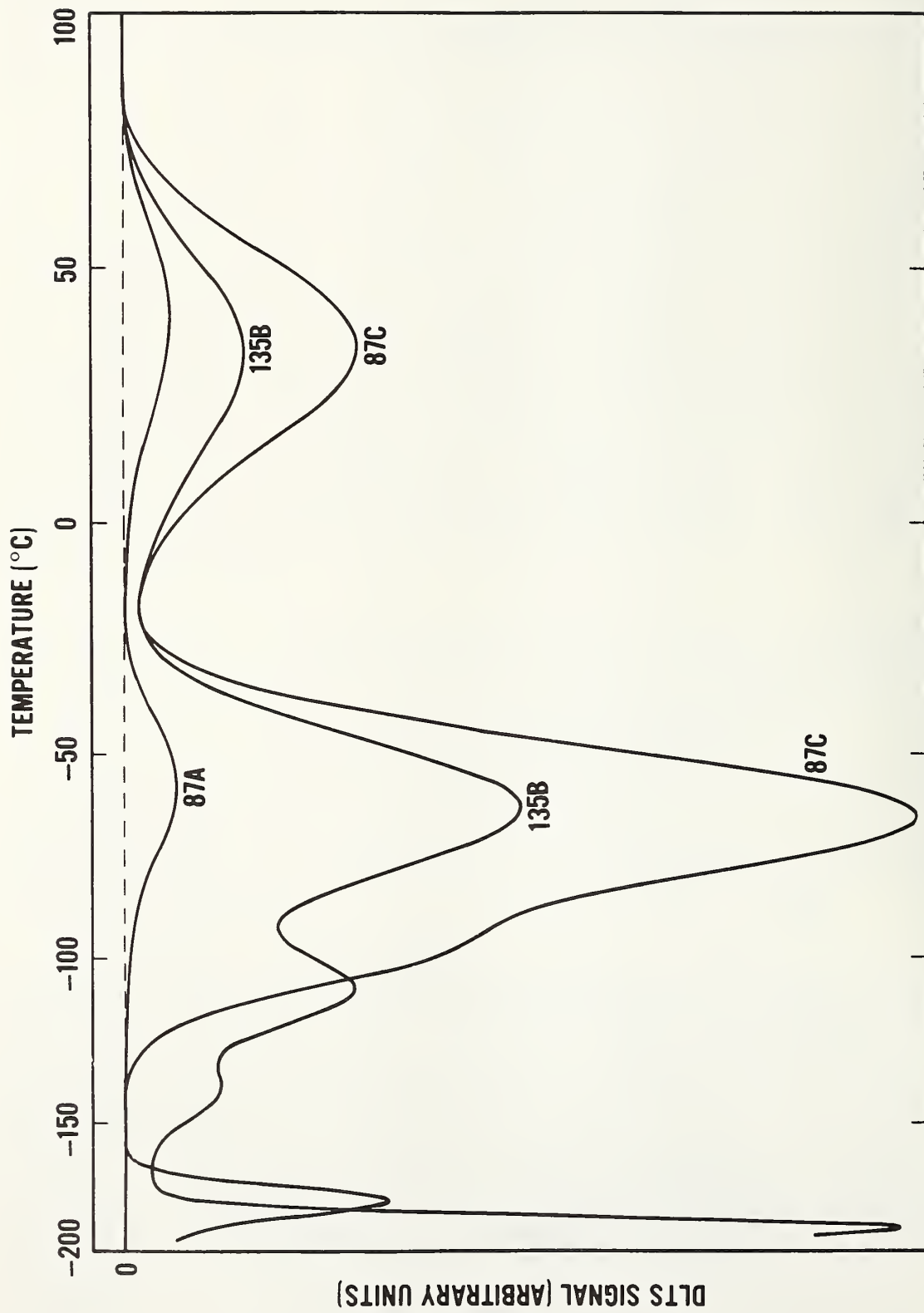


Figure 2-4. Comparison of the DLTS curves of two silicon specimens doped with sulfur by implantation (87A and 87C from fig. 2-2) and one specimen doped by diffusion (135B from fig. 2-3).

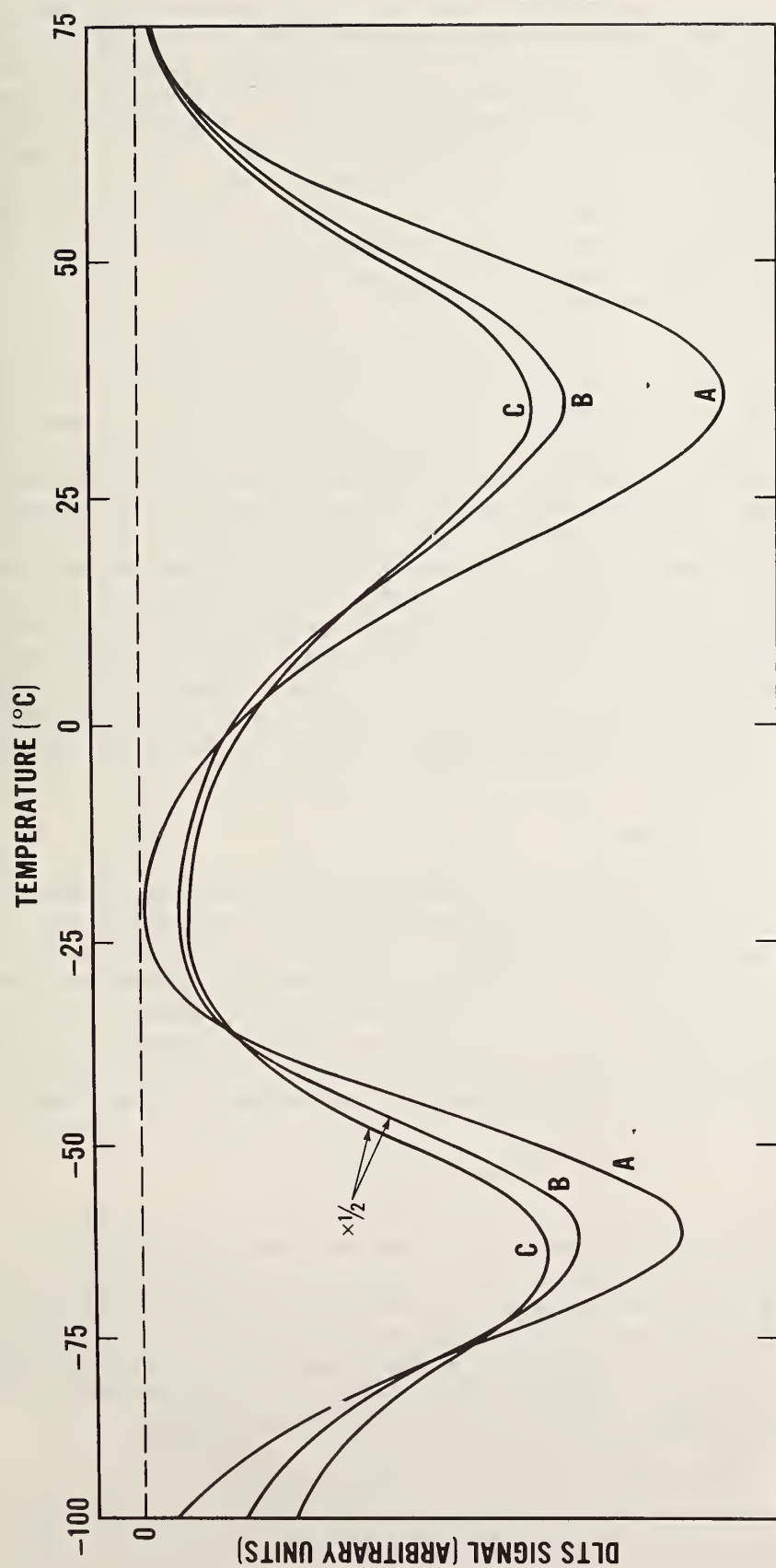


Figure 2-5. DLTS curves showing the effects of annealing on a specimen from wafer 87A. Curve A before annealing; B, after 1 h at 650°C; and C, after 2 h at 650°C. The gate delay times were $t_1 = 251 \mu\text{s}$ and $t_2 = 1015 \mu\text{s}$. The other measurement parameters are the same as those used for the previous three figures.

the intensity of infrared absorption lines with annealing as discussed in section 2.2. The specimen was carefully characterized prior to annealing (curve A). After annealing at 650°C for 1 h in nitrogen (curve B, note scale change), the peak amplitude of both the shallow level (~250 meV) and the deep level (~500 meV) increased by almost a factor of two. This was probably partly due to an increase in the effective junction area caused by the shorting of the guard ring on the device to the junction during the annealing, and partly due to a change in the density of electrically active sulfur. The deep level shifted downward about 1 deg, whereas the shallow level shifted downward 2 deg. The specimen was then annealed another hour at 650°C (curve C). The amplitude of both peaks decreased about 10 percent. The peak position of the deep level remained fixed but that of the shallow level shifted downward three more degrees. After these annealings, the DLTS signal had increased significantly in temperature regions where no peaks are present, particularly at temperatures lower than the peak position of the shallow level. Annealing studies utilizing ITCAP measurements gave analogous changes in emission rate and are reported in section 2.3.2. These studies, which show a shift to lower activation energy with annealing, confirm the effects which were suggested from the infrared absorption experiments outlined in section 2.2. The strongest infrared absorption line, at the highest energy, annealed much faster than the next most intense peak, which was lower in energy. Assuming that the contribution of each state to the effective activation energy is weighted by its density, the effective activation energy should be lower after annealing. Indeed it was found that the DLTS peaks shifted to lower temperatures (decreased activation energies) with annealing. This work was reported in a paper presented at the 1980 Materials Research Society Annual Meeting [2-12].

2.3.1.3 Modeling of DLTS Curves

A possible interpretation suggested by the infrared absorption study is that, instead of a single sulfur center, each DLTS peak represents a group of sulfur-related centers differing slightly in energy. If this is true, then the DLTS peaks should be wider than for a single center because the electron emission comes from centers with a spread in activation energy. To test this interpretation, a model of the DLTS curve shape was developed for single levels in order to compare with the experimental curves. In this model, the emission rate for electrons, e_n , was assumed to have the simple form [2-6, 2-13, 2-15]:

$$e_n = B_n T^2 \exp(-\Delta E_n/kT), \quad (2-1)$$

where T is the absolute temperature, k is the Boltzmann constant, ΔE_n is the energy separation of the deep level in question from the conduction band edge, and $B_n T^2$ is a factor containing the electron capture cross section, electron thermal velocity, and the density of states at the conduction band edge. The factor T^2 in the expression $B_n T^2$ is based on the thermal velocity varying as $T^{0.5}$ and the density of states at the band edge varying as $T^{1.5}$. The resulting capacitance transient can be modeled by:

$$C_T(t) = [C_f - (C_f - C_i) \exp(-e_n t)]_T, \quad (2-2)$$

where $C_T(t)$ is the measured capacitance as a function of time, t , at the

selected temperature, T , and C_i and C_f are the capacitances at the beginning and end of the transient response. In the DLTS measurement, the transient amplitude is sampled for 5 μ s by the boxcar integrator of figure 2-1 at the two times, t_1 and t_2 , and the difference, $\Delta C_T(t_1, t_2)$, is displayed and recorded as the DLTS signal. Thus:

$$\begin{aligned}\Delta C_T(t_1, t_2) &= C_T(t_1) - C_T(t_2) \\ &= [(C_f - C_i) [\exp(-e_n t_2) - \exp(-e_n t_1)]]_T,\end{aligned}\tag{2-3}$$

and T is slowly varied to obtain the DLTS curve.

To confirm the suitability of the single-level model, the shape of the 200-meV level of platinum in n -type silicon was computed. As shown in figure 2-6, the width of the peak at half maximum of the computer simulation was within 2 percent of the experimental width thus verifying the validity of the single-level model. The model was then applied to the DLTS results obtained on a sulfur-implanted wafer (87A). The comparison of model and experimental results is shown in figure 2-7. For each peak the values of B_n and ΔE_n used to calculate e_n in eq (2-3) were obtained from a conventional Arrhenius plot [2-6] of the DLTS peak positions. For the shallow level, $\Delta E_n = 273.1$ meV and $B_n = 1.949 \times 10^5 \text{ s}^{-1} \cdot \text{K}^{-2}$. For the deep level, $\Delta E_n = 488.7$ meV and $B_n = 1.817 \times 10^6 \text{ s}^{-1} \cdot \text{K}^{-2}$. The experimental DLTS curve in figure 2-7 was obtained with $t_1 = 1234 \mu$ s and $t_2 = 5085 \mu$ s and these values were, of course, used for the computer simulation. The calculated amplitude was normalized to the experimental amplitude of the peaks. The width of the high-temperature (deep-level) peak at half maximum is about 5 percent wider than predicted by the model. The low-temperature peak is about 20 percent wider which suggests that more than one center is contributing to the observed emission from the shallow level. This widening is slightly less than 20 percent as the DLTS signal on the low-temperature side (beyond the region shown in fig. 2-7) of the shallow level peak did not return to the baseline (DLTS signal of zero). Beyond the high-temperature peak, the DLTS signal returned to the baseline. The sensitivity of this technique to possible errors in the measured values of ΔE and B is currently being explored, and additional sulfur-doped specimens are being examined as a test of reproducibility. Until this is done, one cannot attribute the broadening of the experimental curves to the existence of multiple centers.

The comparisons of the shape of experimental DLTS curves with simulations based on a single-level model support the interpretation of the optical spectra of sulfur-doped silicon as arising from a group of closely spaced centers. For the deep level the widening is of the same order as the experimental uncertainty, but for the shallow level the widening is significant. When the experimental DLTS shape and the model calculation do not agree, one should seriously question the validity of characterizing the emission by a single, or unique, set of parameters. Parameters of deep levels obtained from an Arrhenius plot are not necessarily meaningful if the shape of the DLTS curves is not in accord with the model underlying the Arrhenius plot. The information gained from modeling the DLTS curve for sulfur suggests that similar modeling and comparison should be done as a test of variability for other impurity systems.

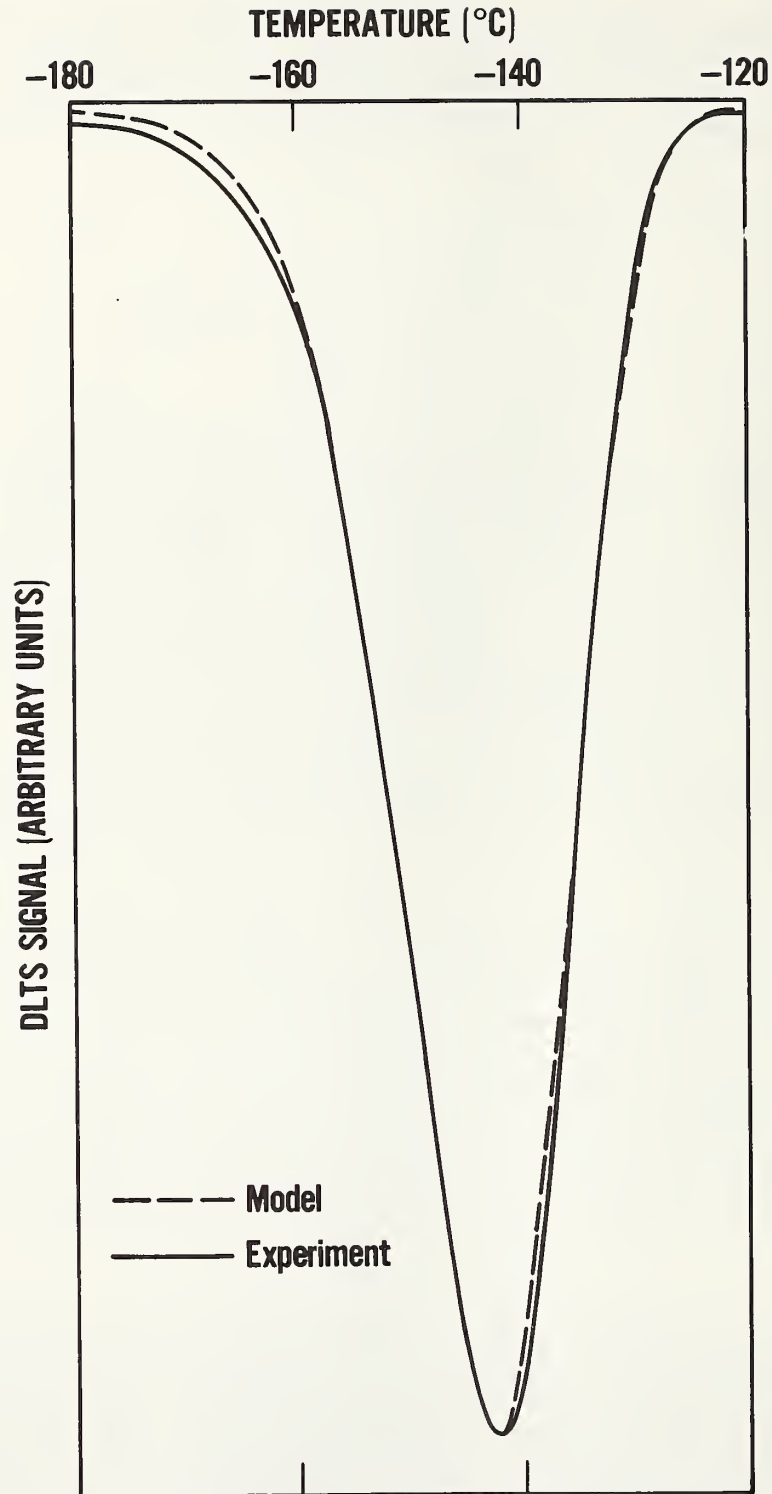


Figure 2-6. Comparison of the calculated experimental DLTS curve for a specimen from an n -type silicon wafer doped with platinum. The gate delay times were $t_1 = 500.5 \mu\text{s}$ and $t_2 = 2055.5 \mu\text{s}$. The emission rate parameters were $\Delta E_n = 196.0 \text{ meV}$ and $B_n = 2.095 \times 10^6 \text{ s}^{-1} \cdot \text{K}^{-2}$.

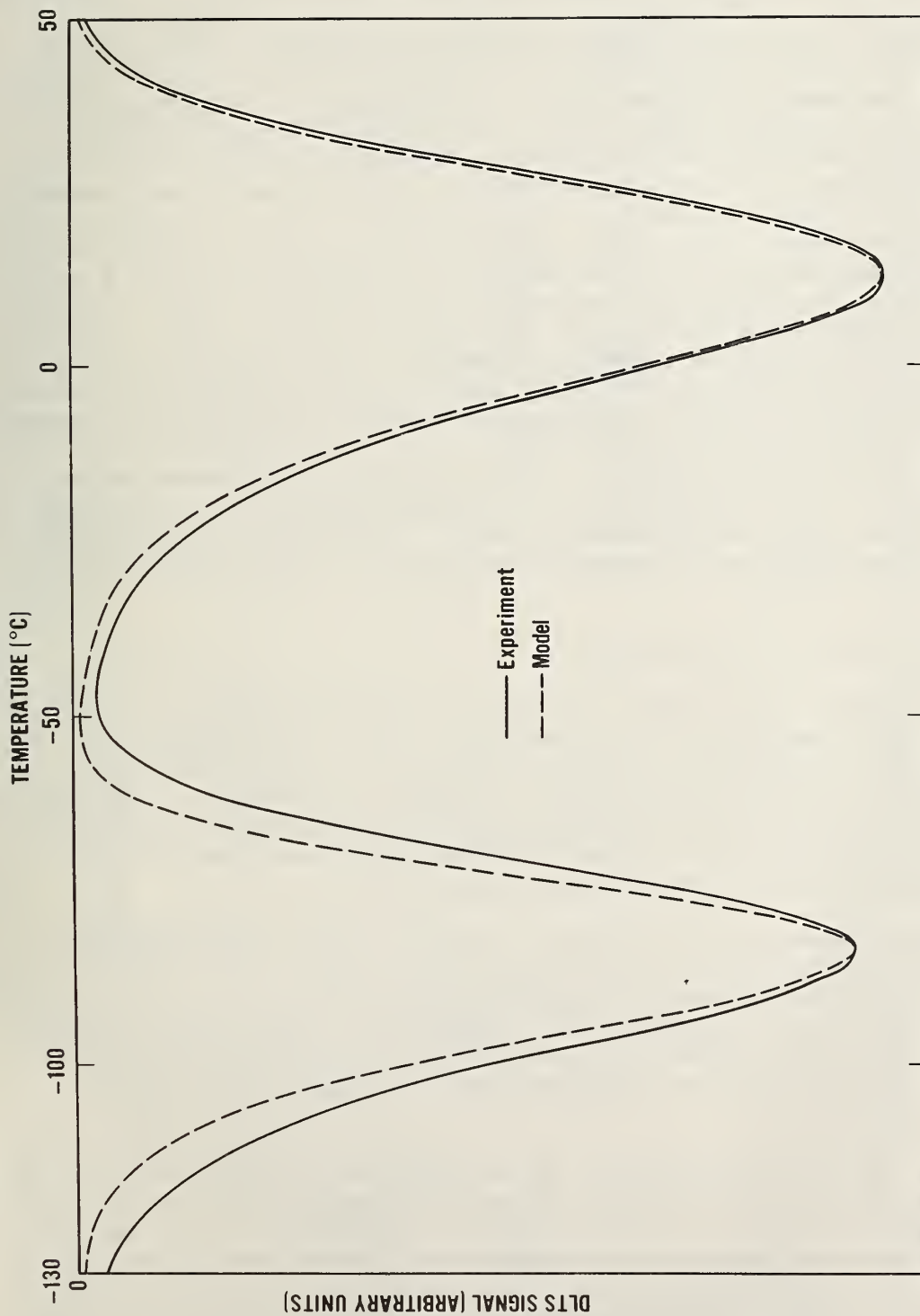


Figure 2-7. Comparison of calculated and experimental DLTS curves for a specimen from wafer 87A implanted with sulfur. The gate delay times were $t_1 = 1234 \mu\text{s}$ and $t_2 = 5085 \mu\text{s}$. The emission rate parameters were $\Delta E_n = 273.1 \text{ meV}$ and $B_n = 1.949 \times 10^5 \text{ s}^{-1} \cdot \text{K}^{-2}$ for the shallow level and $\Delta E_n = 488.7 \text{ meV}$ and $B_n = 1.817 \times 10^6 \text{ s}^{-1} \cdot \text{K}^{-2}$ for the deep level.

2.3.2 Isothermal Transient Capacitance Measurements

Isothermal transient capacitance (ITCAP) measurement techniques are similar to DLTS measurements in that both are based on the same basic phenomena. Both measurements involve the rates of thermally stimulated emission from electrically active defect centers as a function of temperature. The ITCAP measurements complement DLTS measurements in that they are made with greater precision and at a somewhat lower temperature range with slower emission rates. The principal limitation of the present NBS DLTS measurement facility is temperature uncertainty and the use of only two points on the transient capacitance curve (i.e., t_1 and t_2). The temperature uncertainty is reduced in ITCAP measurements by making the measurement under more carefully controlled isothermal conditions and by measuring the temperature with a sensitive, calibrated, temperature-sensing diode in good thermal contact (mounted in the same package) with the specimen diode being characterized. The whole transient is digitized and analyzed in a computer by techniques that make fewer assumptions than in the DLTS technique. The DLTS method is much easier and less time-consuming to use than the ITCAP method because the DLTS method can be used on unpackaged wafers and does not require calibration of temperature-sensing diodes. However, the cost of this ease in use is decreased precision (due mainly to trading good thermometry for expediency). Both systems have their sphere of application - DLTS for a rapid survey of the situation and ITCAP for a detailed analysis of the properties of each deep-level defect center.

2.3.2.1 Description of ITCAP System

A schematic diagram of the present system for ITCAP measurements is shown in figure 2-8. The components shown in the system other than the header are all readily available commercially. A ten-pin package (a TO-100 base with a TO-5 cap) contains the specimen under test and a temperature-sensing diode mounted on a ceramic chip mounted on the base as described previously [2-13]. The specimens under test were fabricated by the implantation-predeposition technique described by Myers, Koyama, and Phillips [2-7].

The package is mounted in an isothermal cryostat as described in NBS Spec. Publ. 400-26 [2-14] except that the heat sink was made larger to provide much better thermal contact between the heat sink, the package, and a dual thermocouple. The dual thermocouple provides an input to a temperature controller for the heat sink and an input to a temperature indicator which is used as a monitor for the more sensitive temperature-sensing diode in the specimen package.

Detailed derivations and description of the measurement method were reported in a previous annual report [2-15]. In order to improve the accuracy (agreement with a "true" value) of the thermometry to reach the desired precision of 0.02 K, a platinum resistance thermometer was acquired and has been calibrated by the NBS calibration service. A transfer calibration system was designed and fabricated and is being tested for use in calibrating the very sensitive but variable temperature-sensing diodes, but is not in routine use at this time.

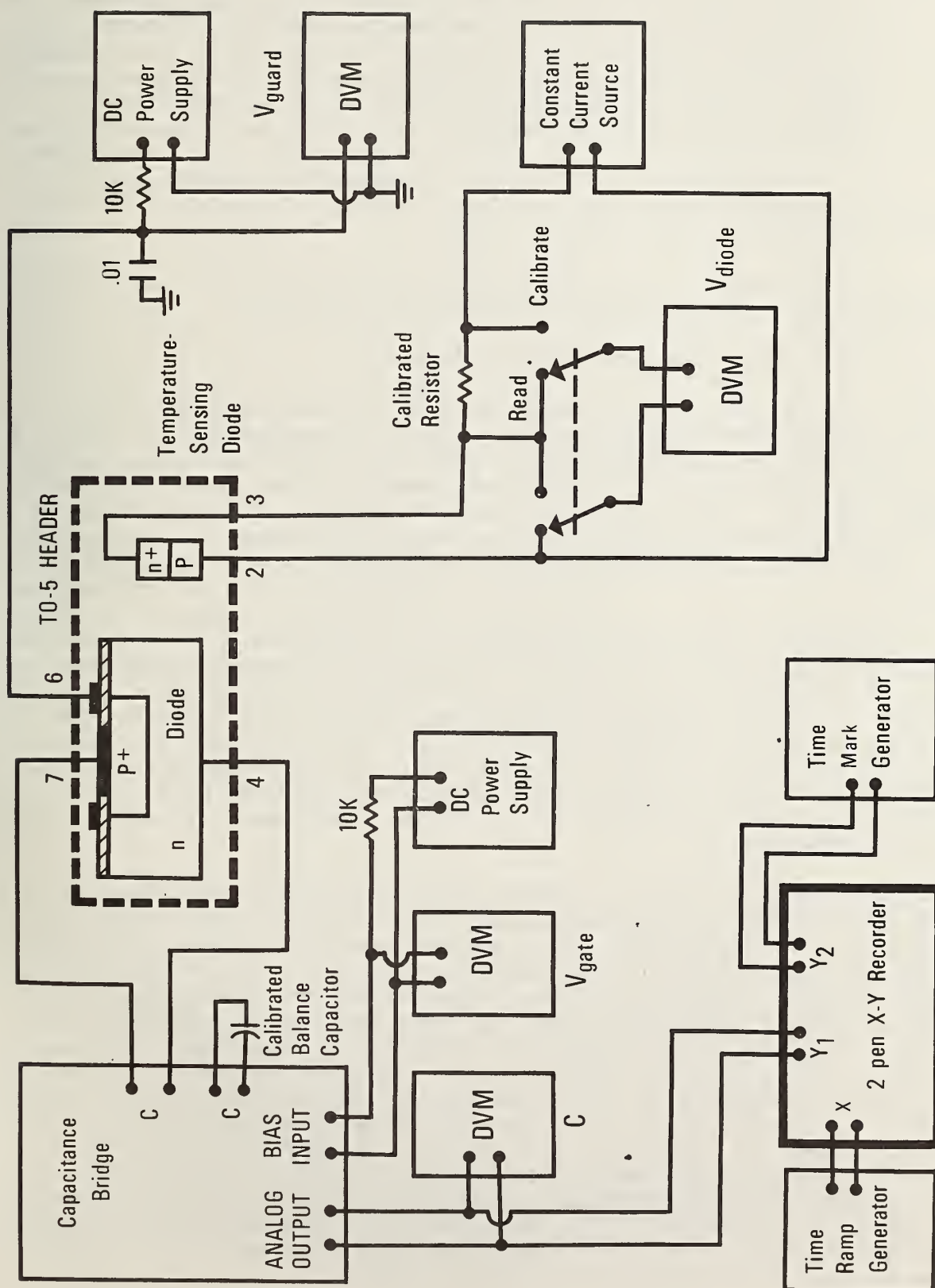


Figure 2-8. Schematic diagram of ITCAP system. Resistance values are in ohms and capacitance values are in μF .

In order to improve the ITCAP system further, a capability for digitization of the capacitance transient was added to the ITCAP measurement procedure. In addition, improvements were made in the computer analysis of the data to correct for the finite response time of the x-y recorder and to use a statistically weighted least-squares regression analysis of the capacitance transient to obtain its time constant (the reciprocal of the emission rate). Correction for the finite recorder response time is made by extrapolating the first seven digitized points back to time zero (the time at which the depletion region is reestablished). The computer-assisted digitization and extrapolation is statistically superior, is more than ten times faster than the manual procedure, and is less prone to error.

The ITCAP system shown in figure 2-8 and operated as described above was used for all the ITCAP results reported in the following section.

2.3.2.2 ITCAP Measurements of Sulfur-Doped Silicon

In order to validate the improvements in the ITCAP measurement method and also to characterize the sulfur defect center in silicon further, a series of experiments on sulfur-doped silicon was undertaken. The disagreement between optical [2-5] and electrical [2-1,2-2] measurements of the energy-level difference between ^{32}S and ^{34}S levels in silicon raised questions about the exact origin of this difference. Several possibilities exist: (1) measurement error, especially in temperature; (2) difference in the implantation densities of ^{32}S and ^{34}S ; (3) variations in annealing of ^{32}S and ^{34}S devices; (4) differences in electric field levels in the depletion layer of the ^{32}S and ^{34}S devices at the time of measurement; (5) variations in density of the postulated complexes in the ^{32}S and ^{34}S specimens; (6) unknown variations in wafers used for ^{32}S and ^{34}S implantations and their processing into test devices; (7) different spatial distributions of ^{32}S and ^{34}S in the diodes; (8) an isotopic mass difference; (9) implantation beam contaminants; and (10) unannealed implantation damage to the lattice. The first five are dealt with in section 2.3.1 and in the following paragraphs. Specimens are being fabricated to eliminate the variability in (6). The other possibilities are discussed elsewhere [2-2].

Improvement in the accuracy of temperature measurements has been a major concern for precision deep-level measurements. Analysis of the thermal properties and expected heat flows predicted that there should be no significant thermal gradients within the ITCAP package. However, an experiment to search for any significant difference in the temperature of the device under characterization and the temperature sensor was conducted. In that experiment two additional temperature-sensing diodes were mounted on the corners of a ceramic chip in a TO-5 header. These diodes were calibrated in the ITCAP cryostat over a range of temperatures. The specimen was rotated 180 deg and the calibration was repeated. The indicated temperature differences over the ceramic chip were within the statistical uncertainty of the calibrations (0.02 K). It was concluded that any temperature difference between the ITCAP specimen and its companion temperature-sensing diode is less than could be measured. This conclusion is consistent with theoretical calculations based on thermal conductivity values of the high-conductivity copper heat sink and radiation values for the cryostat under worst-case conditions.

Previous ITCAP measurements were made on devices with different but individually calibrated temperature-sensing diodes mounted in the TO-5 package with the ITCAP device. However, for an experiment to compare ^{32}S and ^{34}S implanted devices, these two ITCAP devices were mounted in the same header package so as to share a common temperature-sensing diode. This dual specimen package was used for exploratory investigations of emission rate variations with average electric field strength, with distance from the junction interface, and with annealing, and to determine if such variations are different in the ^{32}S and ^{34}S devices.

In order to investigate any spatial variation of emission rate of the sulfur defect center in silicon, a series of ITCAP measurements was made on the deeper sulfur level of these ^{32}S and ^{34}S implanted specimens. The temperature was fixed at 204.9 ± 0.05 K during each recorded ITCAP transient in this series of measurements. Any Poole-Frenkel electric-field effect, if present, was eliminated by making the individual capacitance transient measurements with the same electric field strengths and with the same width of the active portion of the depletion layer. This was accomplished by applying a reverse bias of 5 V to the specimen diode, waiting for equilibrium conditions, partially collapsing the depletion region by reducing the bias to 0 V, waiting a few seconds for the traps in the previously depleted region to fill with majority carriers, then restoring the depletion bias to 5 V. The capacitance transient response was recorded on an x-y recorder during and following these bias changes. The transient response was analyzed to obtain the emission time constant (reciprocal of the emission rate).

The next phase of the measurement was made at a greater average distance from the junction by increasing the initial 5 V of depletion bias, but maintaining the same width of the active region (i.e., the region filled with majority carriers). This was accomplished by making the charging bias, V_C , in volts and the reverse depletion bias, V_R , in volts obey the equation: $\sqrt{V_R} - \sqrt{V_C} = \sqrt{5}$. This equation assumes an abrupt junction for which the total depletion depth varies with the square root of the bias voltage. The constant difference of square roots produces an active region of constant width but at various distances from the junction. The voltage across this active portion of the depletion region remains constant at 5 V as V_R and V_C (and thus the depth) changes. The series of such measurements on the ^{34}S specimen is shown as the top dashed curve in figure 2-9 for a range of uncollapsed depletion biases between 5 and 20 V plotted against average depth of the active region at each bias condition. The series of measurements under the same conditions on the ^{32}S specimen is shown as the bottom dashed curve in figure 2-9. This series of measurements was repeated at a lower average electric field strength on the ^{32}S specimens by using bias voltages in the range of 2 to 20 V and at each step maintaining the relationship: $\sqrt{V_R} - \sqrt{V_C} = \sqrt{2}$ (i.e., 2 V across the active region). This series of measurements is shown as the center solid line in figure 2-9.

The depletion depth, d , was calculated from the measured capacitance, C , at each value of V_R and V_C as $d = \epsilon A/C$, where ϵ is the permittivity of silicon, and A is the area of the junction in SI units. The depletion depth used in figure 2-9 is the value of d at each value of V_R .

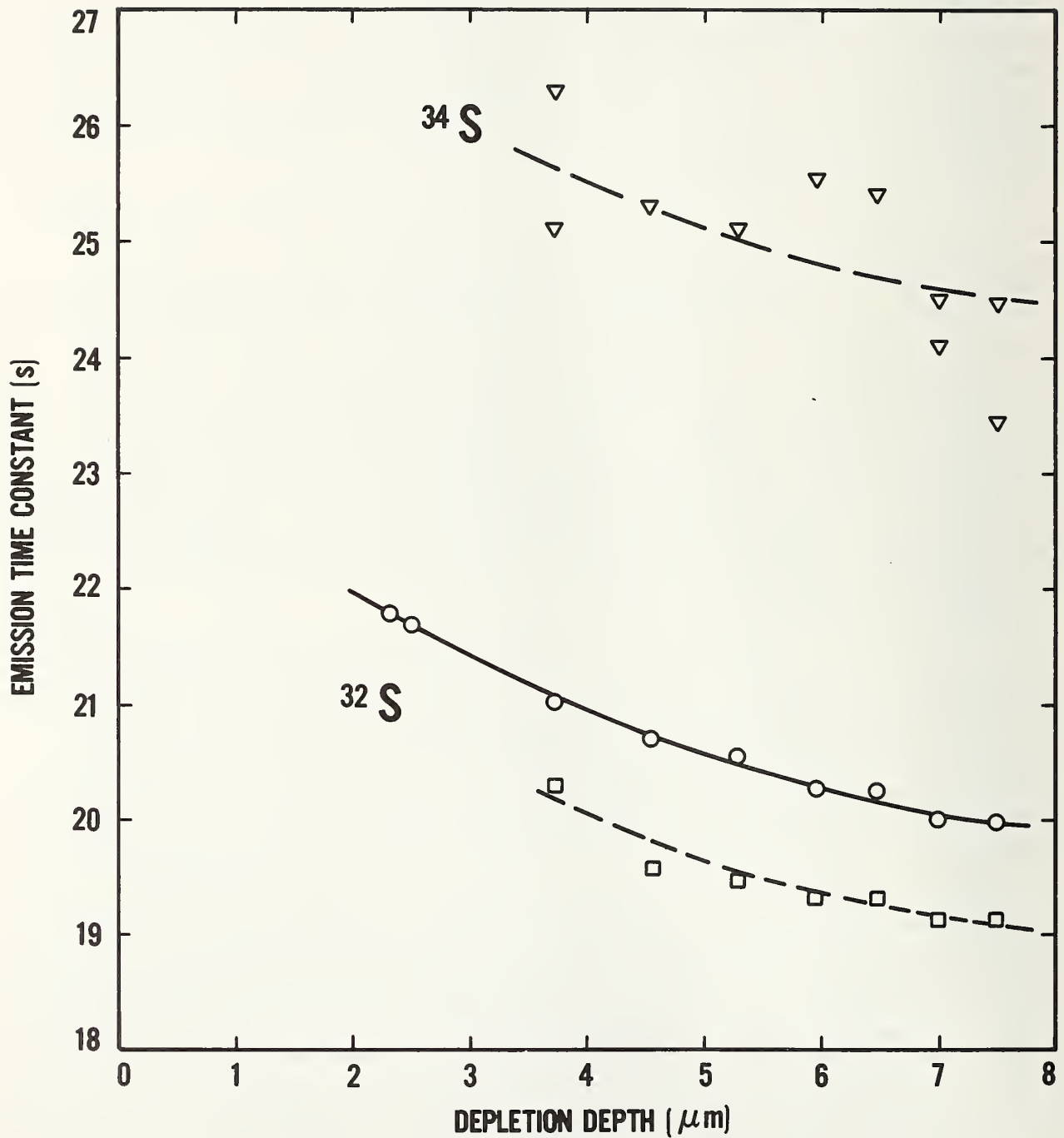


Figure 2-9. ITCAP emission time constant (reciprocal of thermal emission rate) as a function of distance from the diode junction for ^{34}S and ^{32}S defect centers at two different average electric field densities. Dashed lines are for the larger average electric field strength and have the shape of the statistically superior solid line (Device No. 8).

A small (10-percent) spatial variation was found in each specimen (variation from end to end of each line in fig. 2-9). A smaller (5-percent) variation with electric field strength (shift in the bottom two curves) was found for an increase in average electric field strength. A large (40-percent) variation of emission rate between the specimens implanted with ^{32}S and with ^{34}S was found (shift in top and bottom curves). It can be seen that the large isotope-related difference is too large to be readily accounted for by space or field variations.

In order to investigate the possibility that the large isotopic variation is due to the effects of slight processing differences upon various sulfur complexes rather than to the effects of isotopic mass differences *per se*, an annealing experiment was conducted. Although the optical measurements indicated a very small sulfur isotope-related variation of energy levels, they also revealed the existence of several levels spanning a range that could give rise to the variations observed by ITCAP measurements. If it is speculated that the manifold of levels is caused by perturbations of the sulfur level by various sulfur complexes, it is reasonable to expect these complexes to behave differently with annealing. Gettering effects near the junction would also influence the relative densities of these complexes as a function of distance from the junction. Variations in the relative densities would vary the composite emission rate in both ITCAP and DLTS measurements and a manifold of levels would broaden the DLTS peak in comparison with that of a single level.

In this annealing experiment, the ^{32}S and ^{34}S specimens were mounted by indium solder and the temperature-sensing diode was mounted with gold eutectic. Both sulfur-doped specimens were measured, demounted, annealed at 550°C for 5 h, remounted, and remeasured. Capacitance transient responses at 129.8 K for the shallow ^{32}S level before and after annealing are shown in figure 2-10. The time constant before annealing was 9.7 s for a wide range of bias voltages (up to 20 V), indicating that no detectable electric field dependence was present over this range of bias voltages. After annealing, the time constant decreased by 16 percent to 8.1 s. Unfortunately, the guard ring and plate of the capacitor shorted during anneal, thereby adding the MOS guard ring capacitance in parallel with the junction capacitance. (Measurements on similar devices have shown no change in time constant with change in junction size.) Similar changes in the time constant were observed for the deeper ^{32}S level with annealing, but the changes were less pronounced.

It can be concluded that the emission rate is significantly dependent upon the annealing history of the sulfur defect center in silicon. This result adds support to the postulated existence of sulfur-related complexes in silicon. The ITCAP measurement results are in agreement with the DLTS and optical measurement results. They demonstrate the usefulness, precision, and limitations of the measurement methods and indicate the need for similar measurements on other defect centers.

2.4 Conclusions and Recommendations

The present ITCAP and DLTS results have shown that the thermal emission rate (the basic parameter commonly used to characterize deep levels and derive their activation energies and carrier-trapping properties) is not necessarily

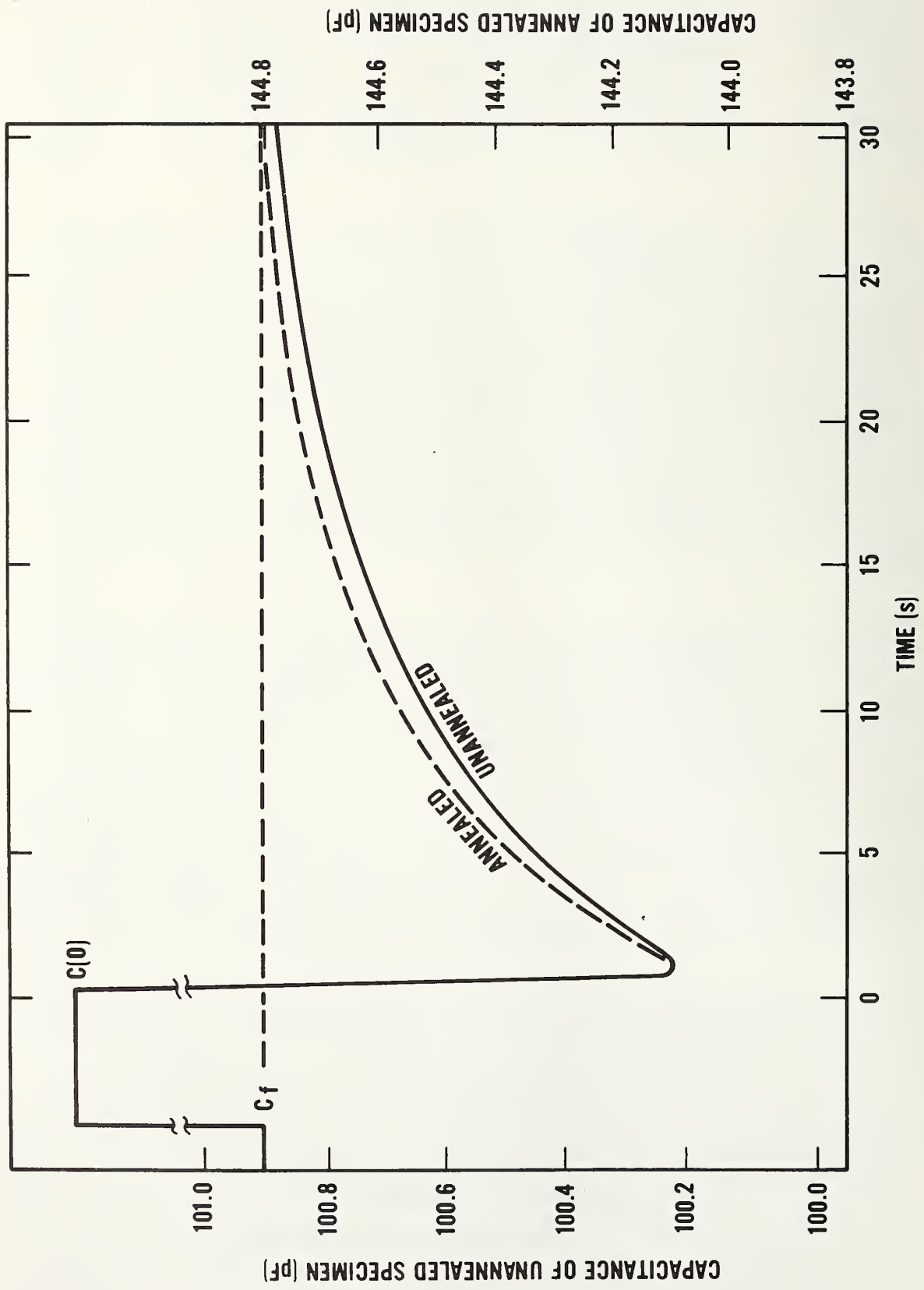


Figure 2-10. ITCAP response at 129.8 K for a 32s implanted diode before and after annealing for 5 h at 550°C (Device No. 5).

a unique property of the levels observed in sulfur-doped silicon. This work has shown that the thermal-emission rate is a function of the depth below the p - n junction of the test device and is also a function of thermal processing and sulfur density used in the fabrication of the test device. The variability with position and thermal history is not expected for a single well-defined energy level in a semiconductor. The present results, coupled with Forman's infrared absorption studies [2-5], demonstrate that the traditional view of the sulfur levels as arising from a simple substitutional sulfur double-donor is not correct. The optical work has led to a model that attributes these variability effects to the presence of a manifold of sulfur-impurity or sulfur-defect complexes with energy levels sufficiently close that they are not resolved in the electrical measurements [2-5]. This hypothesis is consistent with the preliminary results of modeling the shape of DLTS curves. Since such impurity complexing is more likely to be the rule rather than the exception, this situation may not be unique to sulfur. At the present time, it is not known how extensive these variability effects are, and every level must be suspect. If these variability effects are widespread, it may impact the significance, understanding, and value of deep-level measurements for many applications.

It is recommended that these optical, DLTS, and ITCAP techniques be applied to the more interesting (from a practical point of view) dopants such as gold and platinum to determine if these impurities also show variability as a function of annealing, depth, and deep-level density. Levels that exhibit variability are candidates for studies of complexing behavior, while those that do not are candidates for a standard reference material, for use as a standard deep-level specimen, and for initial entries into a catalog of deep-level properties. The experience gained in studying the variability of sulfur-, gold- and platinum-doped silicon will also provide a foundation for the development of recommended procedures for routinely testing for variability in deep-level measurements of any impurity-related center. Some tentative results obtained to date indicate that platinum may introduce such a nonvariable level into silicon. If future experimentation proves this to be the case, platinum-doped silicon will become a very interesting system to study for a number of theoretical and practical reasons.

3. CORRELATION TO DEVICE PERFORMANCE

3.1 Task Objectives

Deep-level defects in the silicon bandgap play an important role in determining the behavior of high-power devices. Impurity-related defects can be added intentionally (e.g., to control switching speed) or can result from contamination contained in the starting material or introduced during the crystal growth process or during high-temperature device processing operations. In any event, impurity-related defects can control the minority-carrier recombination lifetime in the active regions of bipolar devices. In this way, they can affect such electrical parameters as reverse leakage current, forward voltage drop, and switching speed. Therefore, it is important to understand the nature of these lifetime-controlling defect states and their effects on the relevant device parameters.

Traditional transient-capacitance techniques such as DLTS and ITCAP measure the emission properties, rather than the recombination properties, of deep levels. Therefore, some modeling is necessary to relate the measured thermal emission properties to the desired recombination properties such as the carrier capture cross sections and thermal activation energies of the recombination centers. Since this modeling will necessarily involve assumptions and simplifications, it is not a foregone conclusion that the results will adequately relate the thermal emission results to the carrier recombination properties. This has been one factor limiting the utilization of deep-level techniques in industry and motivating a search for ways to measure recombination properties directly.

The emphasis of this continuing task is to test the depth of understanding that has been achieved by determining the degree of correlation between the results of deep-level measurements *per se* and the results of modeling the behavior of excess-carrier recombination lifetime as a function of the measured transient-capacitance thermal-emission parameters. The ultimate goal is the establishment of better techniques for utilizing the results of deep-level measurements for device diagnostic and process-control purposes.

3.2 Background

Previous work [3-1] has demonstrated a correlation between the measured density of deep levels due to intentionally added gold and the reverse-leakage current and the forward-voltage drop of DLTS test diodes. The subsequent efforts have been directed at demonstrating this correlation quantitatively in real device material. Measurements of several lifetime-related parameters of the diodes on unscribed commercially prepared power rectifier wafers showed considerable variation with position over the surface of the wafers and from wafer to wafer [3-2,3-3], thus indicating some degree of nonreproducibility and lack of control. The corresponding DLTS measurements on the same diodes exhibited a series of overlapping peaks and, for the case of the deeper levels, exhibited behavior which was not understood [3-3]. Subsequent work has resulted in a proposed explanation of this unexpected behavior and will be reported below. The problem of resolving these DLTS curves into their component peaks of individual energy levels is being approached by

curve-fitting techniques using the DLTS curve-simulating program discussed in section 2.3.1.2 and will be reported in a subsequent annual report.

The theoretical background for writing a computer program for modeling the excess-carrier recombination lifetime in multilevel systems has been formulated. This program is being designed to accept the density, activation energy, and carrier cross sections of all the states in the bandgap and then to predict the excess carrier lifetime. In order for the predicted lifetime to agree with the measured lifetime over a range of experimental conditions, it is necessary that: (1) the techniques used to measure the thermal emission rates and the models used to convert them to activation energies and capture cross sections be adequate for lifetime-related applications, (2) the deep levels be adequately characterized by the measured deep-level parameters, and (3) the technique selected to measure the lifetime produce meaningful results. If the predicted and measured values of lifetime disagree, it would indicate that one or more of these factors is not true or is not completely understood. It is believed that a study of this kind, directly demonstrating the utility of deep-level measurements to lifetime determination in actual device material, is one necessary prerequisite for a more widespread acceptance and use of deep-level measurements by the power device community.

3.3 Accomplishments During Reporting Period

3.3.1 DLTS Measurements of High-Voltage Rectifier Material

Figure 3-1 shows a measured DLTS curve for a typical mesa-diode device commercially fabricated on a wafer of high-resistivity n -type silicon for use as a high-voltage rectifier. The results of mapping the distribution of the amplitude of the two lowest temperature peaks of this curve over the surface of the wafer were discussed in last year's Annual Report [3-4]. At that time, it was observed that the distribution of the amplitudes of these two peaks over the wafer surface did not match the distribution of several lifetime-related parameters, thus indicating that the levels represented by these peaks are not playing a dominant role in excess-carrier recombination. This could result from the fact that these shallower levels are not present throughout the bulk of the device, are not as effective a recombination center as one or more of the deeper levels, or in the case of the larger of these two peaks, could result from the fact that two overlapping peaks are present and the peak height of the composite DLTS curve is not representative of the density of either level individually. This latter situation can be circumvented by finding a way to resolve the overlapping peaks, mapping their individual amplitudes separately over the wafer surface, and comparing with the corresponding maps of lifetime-related parameters. Overlapping peaks may not be noticeable, but still can give rise to all of the variability phenomena discussed in section 2 above. Therefore, in the absence of confirming evidence, it cannot *a priori* be assumed that any DLTS peak is due to a single level or that its role in excess-carrier recombination can be ruled out by a lack of correlation between the distribution of peak height and the distribution of lifetime-related parameters over the surface of a wafer. Only peaks that can clearly be shown to be attributable to single levels can be used to determine the density, activation energy, and carrier capture cross sections for that level. Peaks that exhibit variability effects such as shown above

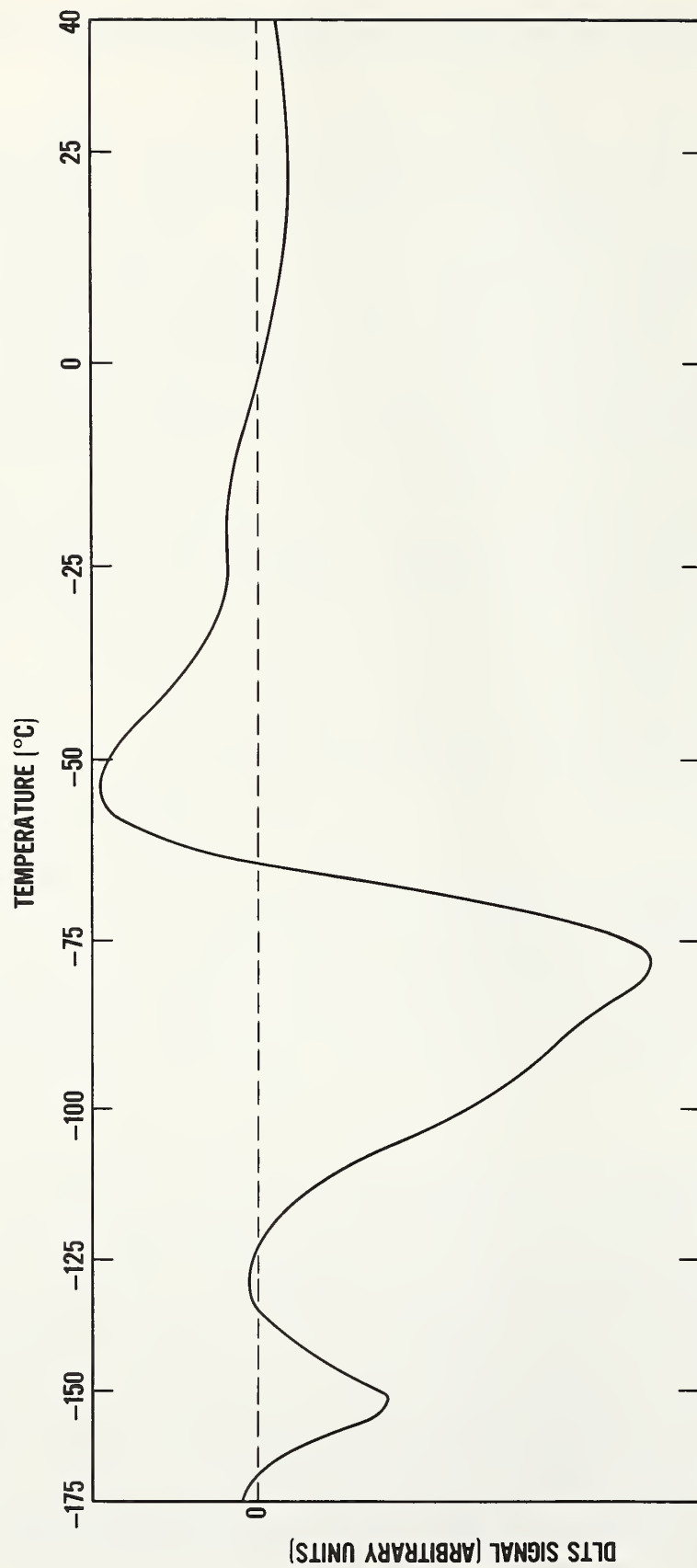


Figure 3-1. DLTS curve of a p - n junction test diode fabricated on n -type high-voltage rectifier material. The gate delay times were $t_1 = 470 \mu\text{s}$ and $t_2 = 961.5 \mu\text{s}$. The reverse bias during the transient was 5 V.

for sulfur-doped silicon, or that are obviously due to unresolved peaks, cannot be used for these purposes with any assurance that the results will have physical significance. Therefore, the current efforts are being directed at first resolving the obvious overlapping peaks in figure 3-1 and then testing for variability effects in each peak separately using the techniques discussed in section 2. The results of this ongoing study will be reported in a subsequent annual report.

The behavior of the DLTS curves of figure 3-1 at temperatures higher than the two lowest peaks is not typical of DLTS curves of majority carrier traps. The junction of the test device was not forward biased during the trap-filling phase of the DLTS measurement cycle, and thus one would expect the deep levels to be filled with only majority carriers (electrons in this case). Consequently, during the subsequent capacitance transient phase, the deep levels could only emit electrons and, under the present sign conventions, produce only negative peaks in the DLTS curve. However, as the temperature of the test specimen is raised above -70°C , the DLTS curve of figure 3-1 passes through zero (i.e., no observable capacitance transient) and becomes positive (i.e., transient capacitance decreasing with time instead of increasing with time as shown for the case of sulfur-doped silicon in fig. 2-10). The curve then passes through a positive peak and at least one other positive or negative peak before passing through zero and exhibiting at least one more low amplitude negative peak. A positive peak under the present sign convention indicates minority carrier (hole) emission, but without forward biasing the p - n junction or otherwise supplying minority carriers during the trap-filling phase of the DLTS cycle, it is not obvious how a positive peak could arise. Hole traps on the p^{+} side of the junction will not produce positive peaks because, on this side of the junction, holes are the majority carrier and such majority carrier traps also give rise to negative peaks.

If the positive peak represents a minority carrier (hole) trap on the n -side of the junction, the trap must lie above the Fermi level in order to be occupied by a larger number of holes than electrons during the trap-filling period of the DLTS cycle. If it is above the Fermi level in this n -type material, its activation energy for hole emission into the valence band would be significantly larger than half the bandgap. However, preliminary analysis of this positive peak by conventional techniques (i.e., Arrhenius plots) yields an activation energy of about 350 meV. Since this value is significantly smaller than half the bandgap, it appears improbable that this positive peak represents a hole trap on the n -side of the junction. An analogous argument argues against its being an electron trap on the p^{+} side of the junction.

However, it is possible that this positive peak could represent a hole trap located on or near the surface of the specimen where the active portion of the depletion layer intersects the surface of the mesa-diode structure. If the surface potential depletes the high-resistivity n -type material so as to increase the hole concentration in this region, the resulting band bending makes it possible to have a hole trap situated on or near the surface that is located above the Fermi level and, at the same time, within 350 meV of the valence band.

One additional piece of experimental evidence has been obtained that supports this model. When the gate delay times t_1 and t_2 are made larger, all peaks

shift to lower temperatures (i.e., longer emission times). However, the positive peaks not only shift to lower temperatures, but decrease in amplitude as well. Since the Fermi level is expected to move up in energy as the temperature is lowered, it moves closer to the postulated hole traps and reduces the number of holes acquired during the trap-filling portion of the DLTS cycle, thereby reducing the amplitude of the corresponding DLTS peak. This model of surface, or near surface, hole traps has been tentatively proposed to explain the present positive DLTS signals, and current efforts are now being directed at more fully testing the validity of this explanation.

If this explanation withstands the test of additional experimentation, it will represent significant progress toward understanding the DLTS curve of figure 3-1 for this material. Since understanding is a prerequisite to proper interpretation of the measured data, it will represent an important step toward properly characterizing the various levels in this rectifier material and measuring the parameters needed for lifetime prediction.

3.3.2 Modeling Lifetime in Terms of DLTS Parameters

When a semiconductor is in thermal equilibrium with its environment, every process has an inverse process which occurs at the same rate. Therefore, electrons and holes are continually being created by thermal excitation and are continually recombining at the same rate. These processes create and maintain a thermal equilibrium concentration of electrons and holes in the conduction and valence bands, respectively. Since these concentrations are a function of temperature as well as the density and type of impurities present, it is impractical to provide general tables listing all possible situations that might occur in practice. Therefore, NBS has prepared and published a FORTRAN computer program that will calculate these densities and several other commonly used thermal equilibrium properties of extrinsic silicon [3-5].

When the thermal equilibrium concentration of electrons and holes is perturbed (e.g., by carrier injection or extraction), the rates of carrier generation and recombination will be changed and new steady-state (but not thermal equilibrium) concentrations will be established if the perturbing influence remains constant. The carrier concentrations under the new nonequilibrium steady-state conditions can be expressed in the following way:

$$n = n_e + \Delta n \quad (3-1)$$

$$p = p_e + \Delta p , \quad (3-2)$$

where n and p are the steady-state concentrations of electrons and holes, n_e and p_e are the thermal equilibrium concentrations of electrons and holes for the prevailing temperature and impurity situation, and Δn and Δp are the deviations from these thermal equilibrium concentrations. Notice that Δn and Δp can be either positive (e.g., injected excess concentration of electrons and holes) or negative (e.g., in a depletion region of a p - n junction), but that n and p cannot be negative (i.e., they are > 0).

The characteristic time constant of the decay of excess-carrier concentration (i.e., positive Δn and Δp) back to thermal equilibrium after some source of

excitation or injection is removed will be called recombination lifetime. Recombination of excess carriers is an important mechanism in the turning-off of high power devices and thus the recombination lifetime is one of the first-order device parameters in many practical applications.

Many deep-level states can act as recombination centers by virtue of their ability to capture electrons and holes successively, thus facilitating their recombination. Traditional deep-level transient capacitance techniques measure a characteristic time constant for the thermal emission of carriers out of deep-level recombination centers under nonequilibrium conditions and thus do not measure recombination lifetime directly.

However, the trapping and emission properties of deep levels are related, because in thermal equilibrium the rates of trapping and emission must be equal. Therefore, the traditional approach is to model this dependence [3-6,3-7] and use the resulting analytical relationships to convert the measured emission properties to the corresponding recombination properties (e.g., carrier capture cross section). Since the details of this procedure are open to question for nonequilibrium conditions, there is no guarantee that the results of applying this model lead to an adequate characterization of the deep levels with respect to excess-carrier recombination.

One test of adequacy is to use this procedure to predict the recombination properties of each deep level, using as input data the measured emission properties for each level. The contributions are summed to calculate the recombination from all such deep levels and thereby to predict the net excess-carrier lifetime. Comparison of the predicted excess-carrier lifetime with values actually measured on the same test devices then serves as a stringent test of not only the model used, but of the adequacy of the original transient capacitance characterization parameters which were used as input parameters for the model. If the traditional DLTS parameters are found inadequate, it may be necessary to revamp the model, reexamine our understanding of the interpretation of DLTS curves, or supplement the traditional DLTS technique with one or more direct measurements of recombination properties (e.g., measurement of the carrier capture cross section by analyzing the time dependence of the amplitude of the capacitance transient as a function of the duration of the trap-filling phase of the DLTS cycle).

3.3.2.1 Modeling Excess-Carrier Recombination Through Deep Levels

Transient capacitance techniques can measure the emission properties of individual deep levels under nonequilibrium conditions in the depletion layer of a test device where n and p of eqs (3-1) and (3-2) are essentially zero. If the effects of the nonequilibrium electric field in this depletion layer are known (or can be shown) to have negligible effect on these emission properties, these emission properties should be the same as would exist under thermal equilibrium conditions. If this is true, the detailed balance of flow rates of carriers into and out of the deep level under thermal equilibrium conditions can be used to deduce the corresponding thermal equilibrium recombination properties of the level [3-6,3-7,3-8]. However, because the lifetime will be subsequently measured under nonequilibrium conditions of excess-carrier concentration (i.e., Δn and Δp in eqs (3-1) and (3-2) are positive and nonzero), it is necessary to model this situation in terms of

the thermal equilibrium recombination parameters. The end result of this model will be an analytic expression (or computer algorithm) for computing the recombination lifetime through a deep level as a function of temperature, excess-carrier density, and the emission properties of that level as measured by transient capacitance techniques. Finally, because several deep-level states may make significant contributions to recombination in actual devices, it is necessary to combine the contributions for all pertinent deep levels into a composite recombination lifetime for comparison with experiment.

Ghandhi has presented a concise analysis of the recombination mechanisms involving a single deep level [3-8]. A computer program for lifetime prediction is being implemented following his basic approach. His most general results can be expressed in SI units in the following form:

$$\tau_n = \frac{[\tau_{n_o} (p_e + \Delta p + p_1) + \tau_{p_o} (n_e + \Delta n + n_1)] \Delta n}{(n_e + \Delta n)(p_e + \Delta p) - n_e p_e}, \quad (3-3)$$

$$\tau_p = \frac{[\tau_{n_o} (p_e + \Delta p + p_1) + \tau_{p_o} (n_e + \Delta n + n_1)] \Delta p}{(n_e + \Delta n)(p_e + \Delta p) - n_e p_e}, \quad (3-4)$$

where:

τ_n and τ_p are the recombination lifetimes of excess electrons and holes respectively. If the excess electron and hole concentrations Δn and Δp are zero (i.e., no injected space charge), then τ_n and τ_p are equal and one can define a single excess-carrier recombination lifetime for the deep levels;

n_e and p_e are the thermal equilibrium concentrations of electrons and holes in the conduction and valence bands, respectively; Δn and Δp are the concentrations of the excess (i.e., excess over thermal equilibrium) electrons and holes, respectively; n_1 and p_1 are "fictitious" concentrations of electrons and holes that would exist in the conduction and valence band, respectively, if the Fermi level were located at the same energy as the deep-level recombination center;

τ_{n_o} and τ_{p_o} are characteristic times associated with the capture of electrons and holes by the deep level, and are given by:

$$\tau_{n_o} = \frac{1}{C_N v_t n_t}, \quad (3-5)$$

$$\tau_{p_o} = \frac{1}{C_P v_t n_t}, \quad (3-6)$$

where C_N and C_P are the capture cross sections for electron and hole capture, respectively, v_t is the average thermal velocity of the charge carrier, and n_t is the concentration of the deep-level recombination center.

The algorithms used in the previous NBS evaluation of the thermal equilibrium properties of extrinsic silicon [3-5] can be used to evaluate n_e , p_e , n_1 , and p_1 if the concentration, activation energy, and degeneracy of each state in the bandgap are known. Hall measurements can be used to measure these parameters directly or supply the data necessary to compute these parameters for the shallow dopant levels and the question is: Can transient capacitance techniques be used to measure meaningful values for these parameters for the deep levels? Evaluation of the characteristic times τ_{n_0} and τ_{p_0} of eqs (3-5) and (3-6) requires knowledge of both the electron and hole capture cross sections of each energy level. However, in practice, thermal excitation from the shallow dopant levels is usually fast enough that reemission occurs before recombination and such levels are very ineffective recombination centers. Therefore, the shallow dopant centers need not be considered as participating in the recombination kinetics *per se*, but only as participating indirectly in the determination of n_e , p_e , n_1 , and p_1 . As the energy level of the state moves away from a band edge, the thermal-emission rate at any given temperature decreases and the probability of recombination before reemission increases. When recombination at such sites increases enough to become a significant influence on the excess-carrier lifetime, one or both of the capture cross sections (depending on which is rate limiting) need to be measured. Fortunately, for near mid-gap states, there is a way to separate the electron and hole contributions to the measured DLTS curves [2-1].

In this way, eqs (3-3) and (3-4) can be applied to each deep level in turn and a characteristic recombination lifetime computed for each level (assuming that Δn and Δp are equal in the subsequent measurement of excess-carrier lifetime). These results will not only reveal which level (or levels) have the lowest lifetime and thus dominate the recombination kinetics, but also allow one to evaluate a composite recombination lifetime for the given collection of recombination centers. For low injection levels (where the terms Δn and Δp within the expressions multiplying τ_{n_0} and τ_{p_0} in eqs (3-3) and (3-4) can be ignored) and for the case of present interest where $\Delta n = \Delta p$, it can be shown that the recombination lifetime for each level given by eqs (3-3) and (3-4) becomes independent of the properties of any other levels in the bandgap. In this limit, the effective lifetime for all centers taken collectively is simply the reciprocal of the sum of the reciprocals of the individual lifetimes of the recombination centers as computed by eq (3-3) or eq (3-4). Therefore, it is suggested that any initial attempts at comparing predicted and measured lifetime be conducted in this simpler low injection level regime. After a foundation of understanding and proven adequacy of the deep-level characterization in this regime has been established, it would then be appropriate to consider the more complex case of the higher injection levels of interest in high power devices.

3.4 Conclusions and Recommendations

The present DLTS measurement results on the power rectifier wafer vividly demonstrate that the material actually used in practical devices can exhibit a much more complex behavior than is generally exhibited in specially prepared laboratory specimens that are intentionally doped with a single element. Since DLTS does not unambiguously measure the desired recombination properties directly, it becomes necessary not only to understand and interpret the measured DLTS curves in terms of the deep levels present, but also

to show that the parameters selected to characterize those deep levels are relevant to the performance of devices. The present results show how understanding and interpretation can be clouded by the complexity caused by the number and variety of levels present as well as by nonreproducibility effects such as those seen in sulfur-doped silicon and termed variability in this report. However, despite these pitfalls, the potential value of deep-level measurements is significant. DLTS offers a relatively simple way to obtain information about the recombination centers in a very pictorial (i.e., spectrum-like) way suitable for rapid survey or quality control purposes. It is anticipated that if the practical problems like those outlined above can be solved, circumvented, or even better understood, the present negative onus about deep-level techniques will disappear, and a more widespread utilization of this potentially useful technique will be fostered in areas outside the research laboratory.

4. STANDARDIZATION ACTIVITIES FOR SPREADING RESISTANCE ON THYRISTOR-GRADE SILICON*

4.1 Task Objectives

The ability to measure and to control dopant profiles is important in thyristor structures for a variety of reasons. Perhaps the single most important parameter that is affected by variations in dopant density is reverse blocking voltage which is limited by the lowest local resistivity region of the base starting material. The overall objective of this continuing task is to increase the reliability with which spreading resistance measurements can be used for radial resistivity screening of thyristor material, and, more importantly, for depth resistivity profiling of partially or fully fabricated thyristor structures. The applications for such measurements extends from process control during thyristor fabrication to profile analysis necessary for the design and performance modeling of newer and more advanced thyristor structures.

The current emphasis has been on completing the acceptance procedure for the nonaqueous diamond-polishing techniques developed during FY-1978 and FY-1979 [4-1,4-2] for inclusion in the *Annual Book of ASTM Standards*. In addition, a multilaboratory round robin is being conducted by NBS under the auspices of ASTM Committee F-1 on Electronics as a test of interlaboratory and within-laboratory reproducibility of spreading resistance measurements. These two activities are nearing completion and required considerably less attention than the deep-level work during the present reporting period.

4.2 Accomplishments During Reporting Period

During FY-1980, the formal acceptance procedure within ASTM of the standard practice for preparing high-resistivity n -type silicon for spreading resistance measurements was completed with a Society-level ballot in May 1980. This Standard Practice was published in Part 43 of the *Annual Book of ASTM Standards* [4-3] and has the designation F 674-80. A copy of this Standard Practice is included in Appendix A of this report.

Six of the 15 laboratories participating in the interlaboratory test of repeatability of spreading resistance measurements on bulk silicon specimens have completed and reported their measurements. Analysis of these data, emphasizing repeatability as a function of specimen preparation, is being undertaken under NBS sponsorship, and the results will be included in a future DOE report.

* Report on continuing work of J. R. Ehrstein.

5. OTHER ACTIVITIES RELATED TO DOE-SPONSORED WORK

5.1 Informal Gold-in-Silicon Round Robin

An informal interlaboratory test of deep-level measurements on gold-doped n - and p -type silicon is being conducted by NBS in order to assess the state of the art in deep-level transient spectroscopy (DLTS). Measurements have been completed by six of the eight laboratories who have asked to participate in this test. The techniques of measurement have not been explicitly specified, and the various laboratories have used a variety of techniques including: (1) DLTS with either a box-car integrator or a lock-in amplifier, (2) DLTS with constant reverse-bias voltage or constant depletion layer capacitance, and (3) isothermal transient capacitance (ITCAP). Discussions with the participants have revealed that the measurement of temperature is usually the most significant factor limiting accuracy. In fact, such discussions have resulted in improvements in thermometry being implemented before making the measurements. The values reported to date for the thermal activation energy and concentration of the major deep level in these n - and p -type specimens are given in table 5-1. These results show that if proper attention is given to thermometry, the activation energy for a given specimen can be reproduced to within several percent. Although this may be an adequate level of precision for many industrial purposes (e.g., quality control), it may not be sufficient for many research and development purposes (e.g., showing that two laboratories are actually measuring the same defect state).^{*} A complete analysis of the results of this round robin will be undertaken after all participating laboratories have made the necessary measurements on these two specimens and submitted their results. The final results will be reported in a future DOE report.

^{*} The level of precision reported in table 5-1 requires careful attention to thermometry and was not always obtained. When this level of precision was not obtained, it was recognized and the thermometry improved. As a result, the new results were within this level of precision.

Table 5-1. Reported Gold-in-Silicon Round-Robin Results.

Laboratory	<i>n</i> -type specimen		<i>p</i> -type specimen	
	Activation Energy (meV)	Concentration (cm ⁻³)	Activation Energy (meV)	Concentration (cm ⁻³)
A	530	3.7×10^{13}	340	
B	541		341	
C	550	2.3×10^{13}	360	2.2×10^{13}
D	540	5.0×10^{13}	340	4.0×10^{13}
E	520		345	
F	550			
Average	539 ± 12		345 ± 9	

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If not listed in the current combined index, will appear in the next edition.

Standard Practice for PREPARING HIGH-RESISTIVITY *n*-TYPE SILICON FOR SPREADING RESISTANCE MEASUREMENTS¹

This standard is issued under the fixed designation F 674; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval.

1. Scope

1.1 This practice covers the surface preparation of (111) *n*-type silicon prior to measurement of resistivity variation by the spreading resistance technique.

1.1.1 The procedures given are primarily intended for use with (111) *n*-type silicon specimens with room-temperature resistivity above 1 $\Omega \cdot \text{cm}$ (see 4.2).

1.1.2 The procedure can also be applied to (111) *n*-type silicon specimens below 1 $\Omega \cdot \text{cm}$, and to *p*-type silicon specimens.

1.1.3 Separate procedures are given for preparation of large-area specimens for measurement of lateral resistivity variation and for preparation of bevel-sectioned specimens (usually small chips) for measurement of vertical variation of resistivity (depth profiling).

2. Summary of Practice

2.1 Silicon specimens are polished using fine-grain diamond compound in a non-aqueous fluid. Polishing of silicon slices or other large-area specimens is done against a nonwoven polishing cloth; bevel polishing of small specimens is done against a frosted glass surface. When polishing is complete, residual polishing compound is removed by organic solvent.

3. Significance and Use

3.1 Resistivity is probably the single most important parameter for the characterization of silicon starting material for semiconductor device fabrication. Spreading resistance measurements are used to measure resistivity variation in raw silicon crystals and completed semicon-

ductor devices. The reproducibility of spreading resistance measurements on silicon specimens is known to depend on the manner of specimen preparation. The interpretation of spreading resistance measurements depends in turn on the reproducibility of test specimen measurements and on the reproducibility of calibration specimen measurements.

3.2 The procedures given are intended to confer a high degree of reproducibility to spreading resistance measurements, and offer particular improvement over other preparation techniques on (111) *n*-type material with resistivity above 1 $\Omega \cdot \text{cm}$.

4. Interferences

4.1 Polishing of silicon with diamond causes light but controllable and uniform scratch damage to the silicon surface. Nevertheless, such uniform damage is compatible with spreading resistance measurement data having very low scatter. Contamination of the polishing medium with hard foreign particles can cause random heavy scratch damage to a specimen. If they are encountered by the spreading resistance probes, heavily damaged regions may yield erratic measurement results.

4.2 Contamination of the specimen with water subsequent to polishing may adversely effect the reproducibility of spreading resistance measurements.

¹ This practice is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Electrical and Optical Measurement.

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5. Front-Surface Diamond Polishing

5.1 Apparatus:

5.1.1 *Polishing Machine*—Oscillating-tub polisher or other similar small laboratory-scale polishing machine capable of providing randomized motion of the silicon specimen over the polishing pad.

5.1.2 *Mounting Block and Fixture*, to support and apply vertical load to the silicon polishing during polishing.

5.1.3 *Polishing Pad*—Nonwoven cloth pad of a texture specified as being compatible with the grain size of diamond used during polishing. The polishing pad should be adhesive backed for attaching to the rigid plate.

NOTE 1—The preferred material is of a type identified as a "chemotextile."²

5.1.4 *Rigid Plate*, of glass or other similar hard material compatible with the chosen polishing machine and capable of providing a flat support for the polishing pad during polishing.

5.1.5 *Microscope*—Optical microscope having total magnification of at least 30 $\times$ and system for illuminating stage obliquely.

5.1.6 *Hot Plate* capable of heating the mounting block and wax to 150°C.

5.2 Reagents and Materials:

5.2.1 *Diamond Slurry*—Synthetic or natural diamond with grain size in the range 0.5 to 3 μm , inclusive, suspended in a nonaqueous liquid or paste carrier.

NOTE 2—The predominant causes of variation in the surface finish of the silicon specimen are expected to result from (1) the uniformity of particle size in the diamond grit, (2) the inclusion of a large fraction of needle-shaped grains (fines) in addition to the preferred symmetric grains (blocky diamond), and (3) in the case of diamond suspended in paste, the uniformity of the diamond distribution in the paste. For a fixed diamond grain size, whether the diamond is natural, single-crystal synthetic, or polycrystalline synthetic should make little difference in the resulting surface finish. However, the breakdown mechanisms differ somewhat for the different types of diamond. Consequently, the size and type of diamond should be chosen to give acceptable cutting rate for the specimen and machine conditions that will be used.

NOTE 3—For use with large-area specimens, the appropriate size diamond grain and, in part, the type of diamond to be used should be compatible with (1) the starting surface texture of the silicon, which may range from as-sawn to prepolished, and (2) the load that is applied during polishing.

5.2.2 *Solvent*—Suitable nonaqueous solvent

for removing diamond slurry subsequent to polishing.

NOTE 4—The choice of solvent is governed in part by the composition of the carrier liquid or paste. The supplier of the diamond slurry should be consulted regarding the appropriate solvent. Acetone ($(\text{CH}_3)_2\text{CO}$) and methanol (CH_3OH) are known to work well for removing many commercial diamond compounds.

5.2.3 *Wax*—Glycol phthalate or other similar wax having a melting temperature of less than 150°C.

5.2.4 *Dry Air*—Source of clean, dry air suitable for drying the specimen.

5.3 Procedure:

5.3.1 If not previously done, attach the polishing pad to the rigid plate and place several drops of diamond polishing slurry at random locations on the polishing pad surface. Spread drops of slurry in a reasonably uniform manner over the pad so that the pad surface becomes damp and so that there are no freestanding layers of slurry. If the diamond is suspended in paste, be sparing in the amount of paste applied to the pad.

NOTE 5—Some polishing slurry adheres to the specimen and mounting fixture and is lost every time a specimen is removed and cleaned. Replenish the slurry on the pad regularly with a few drops of fresh slurry.

5.3.2 With the hot plate, heat the mounting block to the melting temperature of the wax. Mount the silicon specimen to the block with the wax. Allow the block to cool to room temperature.

5.3.3 Assemble the mounting block with specimen and the mounting fixture and place this assembly on the polishing pad in the polishing machine.

5.3.4 In accordance with the manufacturer's instructions for the polishing machine, polish until the specimen surface exhibits a uniform density of random-direct scratches comparable to the pattern shown in Fig. 1. For this test, remove the polishing slurry from the specimen

² Pellon Cloth is manufactured by The Pellon Corp., Chelmsford, Mass. 01824 and is also available from suppliers of polishing materials such as: GEOS Corp., Stamford, Conn. 06902 and J. I. Morris Co., Southbridge, Mass. 01550. Kem-pad is available from The Glennel Corp., Chester Springs, Pa. 19425. Texmet is available from Bueler Ltd., Evanston, Ill. 60204.



surface and examine that surface with the microscope.

NOTE 6—The time required to reach a uniform surface finish will depend on specimen surface area, size of diamond grains, static load applied, and rate of movement of the specimen surface over the polishing pad.

5.3.5 When an acceptable surface finish has been reached, thoroughly swab or flush the specimen with the solvent to remove all diamond slurry residues. With the dry air, blow the specimen surface dry prior to carrying out any spreading resistance measurements.

NOTE 7—The coarseness of the scratch damage on the specimen surface is related to the size of diamond grit used.

6. Diamond Bevel Polishing

6.1 Apparatus:

6.1.1 *Glass Plate*, of suitable area for convenient use, which has been given a frosted surface by lapping with water slurry of nominal 5 to 12- μm aluminum oxide, or similar abrasive, and thoroughly cleaned subsequent to lapping.

6.1.2 *Mounting Block and Fixture*, for holding the silicon specimen at the desired beveling angle during the bevel-polishing process.

6.1.3 *Microscope*—Optical microscope having a total magnification of at least 30 $\times$ and a system for illuminating the stage obliquely.

6.1.4 *Hot Plate*, capable of heating the mounting block and wax to 150°C.

6.2 Reagents and Materials:

6.2.1 *Diamond Slurry*—Synthetic or natural diamond with grain size in the range 0.1 to 0.5 μm , inclusive, suspended in a liquid or paste carrier.

6.2.2 *Solvent*—Suitable nonaqueous solvent for removing diamond slurry subsequent to polishing (see Note 4).

6.2.3 *Wax*—Glycol phthalate or other similar wax having a melting temperature of less than 150°C.

6.2.4 *Wipe* of lint-free paper or cloth and suitable for cleaning the glass plate.

6.2.5 *Oil Extender* compatible with the diamond slurry (6.2.1).

6.3 Procedure:

6.3.1 Prior to beveling each specimen, clean the frosted surface of the glass plate by swabbing with the solvent using the lint-free wipe.

NOTE 8—Because of the rigidity of the glass sur-

face, excessive damage to the beveled silicon surface can result from contamination of the polishing slurry with foreign material whose size is larger than that of the diamond grit.

6.3.2 Apply a small amount of diamond slurry (or paste) to the surface of the glass. An oil extender may be used to prolong the life of the slurry. Distribute the slurry (or paste) with a clean cotton swab or other clean, soft applicator so that a thin, uniform film results over an area whose dimensions are several times larger than the lateral dimension of the fixture used to support the beveling block.

6.3.3 Mount the specimen in accordance with 5.3.2.

6.3.4 Assemble the mounting block with specimen and the mounting fixture, and place this assembly on the glass plate.

6.3.5 Polish the specimen by orbital, figure-eight, or reciprocating movement of the polishing fixture over the glass plate.

6.3.6 Clean and inspect the specimen periodically to determine whether an adequate amount of specimen surface has been exposed by beveling.

6.3.7 Repeat 6.3.5 and 6.3.6 as necessary until an adequate extent of beveled surface is obtained.

NOTE 9—At the beginning of the beveling process an extremely small area of silicon supports the static load of the polishing assembly, and pressures on the silicon are extremely high. To minimize the possibility of fracture of the edge of the silicon chip, it has been found advisable to begin bevel polishing with a relatively slow rate of motion of the polishing assembly.

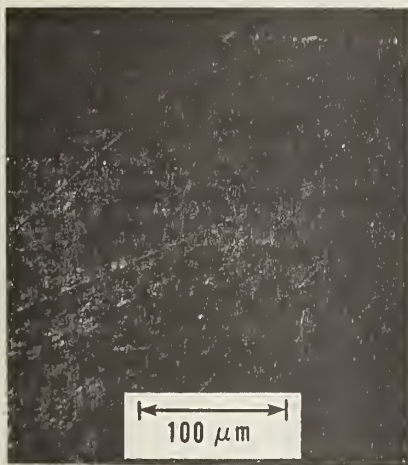
6.3.8 When the desired amount of specimen surface has been exposed by beveling, thoroughly clean the specimen by flushing or swabbing with the appropriate organic solvent. Inspect the beveled surface for quality of finish with the microscope. Compare the finish with the appropriate photograph of Fig. 2, which shows results obtainable with different size diamond in the range specified for two types of motion during polishing. Repolish lightly if the finish appears to be significantly coarser than that shown in the appropriate photograph. With the dry air, blow the specimen surface dry prior to carrying out any spreading resistance measurements.

NOTE 10—The polishing plate should be cleaned

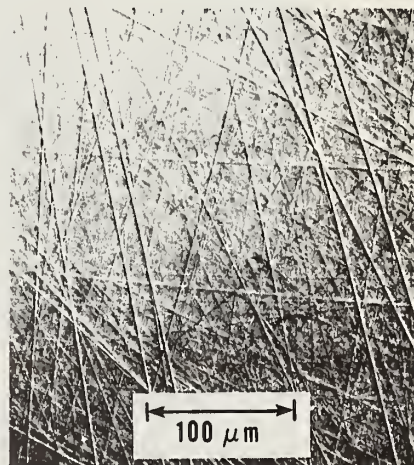


regularly to remove coarse polishing residue or airborne contaminants. This cleaning can be done with a lint-free cloth or paper wipe and the same solvent used to clean polishing residue from the specimen.

The plate should be inspected when clean. If it shows signs of scratching, burnish marks, or areas where the lapped finish has been polished smooth, the plate should be relapped.

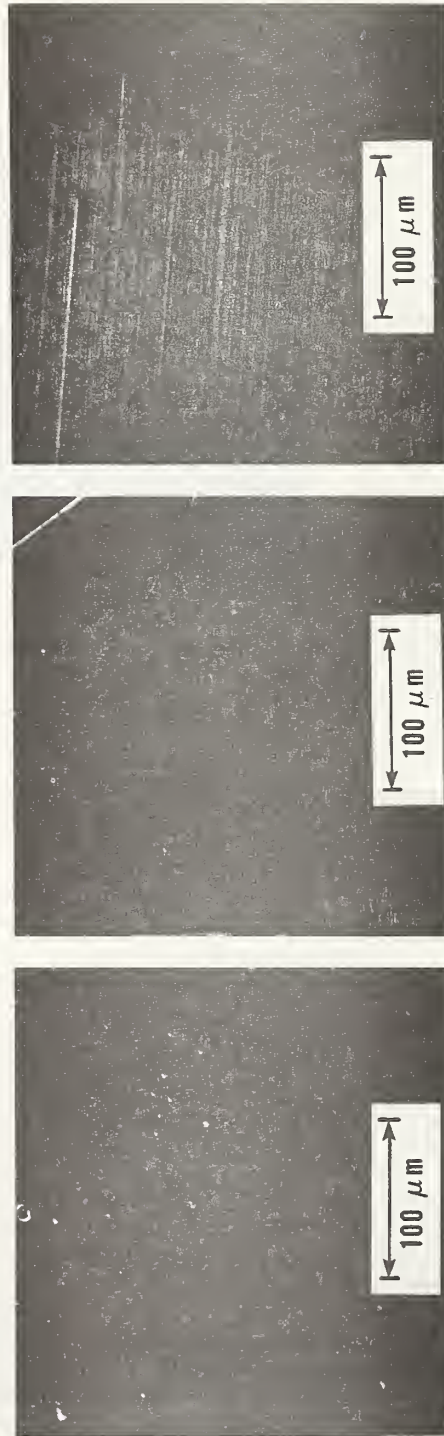


a



b

FIG. 1 Surface Texture of Large-Area Silicon Specimen Polished with Diamond Against Chemotextile Pad (a) 0.5- μm Diamond (b) 3- μm Diamond.



NOTE: Vertical arrows denote edge of bevel; beveled surface extends to left of arrow. Original top surface (to right of arrow) is covered with an oxide layer in (a) and (b) and is bare in (c).

FIG. 2 Surface Texture of Silicon Specimens Bevel-Sectioned with Diamond Against Ground-Glass Surface. (a) 0.1-μm Diamond, Reciprocating Motion; (b) 0.1-μm Diamond, Figure-Eight Motion; (c) 0.5-μm Diamond, Reciprocating Motion.

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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here) The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during crystal growth and during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The effective utilization of deep-level measurements for this purpose requires three things: (1) development of well-characterized measurement and data analysis procedures, (2) characterization of a variety of levels to establish the validity of the techniques and establishing a data bank of the properties of known defect levels, and (3) understanding the relationship between the presence of deep levels and the corresponding device parameters. Efforts in deep-level metrology during the present reporting period were concentrated specifically on the first and third of these basic requirements. This effort is divided into two ongoing tasks concerned with (1) the introduction of specific impurities into silicon wafers and the characterization of the resulting deep levels and (2) the correlation of the results of these deep-level characterization techniques with the electrical properties of devices. A third task concerned with the standardization of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon was essentially completed during the year.				
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